Trials@uspto.gov
571-272-7822

Paper 10
Date: May 4, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

IPR2023-00130
Patent 7,116,710 B1

Before KEN B. BARRETT, JOHN A. HUDALLA, and AMBER L. HAGY, *Administrative Patent Judges*.

HAGY, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition requesting *inter partes* review of claims 11–17 and 19–33 of U.S. Patent No. 7,116,710 B1 ("the '710 patent," Ex. 1001). Paper 1 ("Pet."). California Institute of Technology ("Patent Owner") filed a preliminary response to the Petition. Paper 7 ("Prelim. Resp."). With our authorization, Petitioner filed a Preliminary Reply (Paper 8, "Pet. Reply") and Patent Owner filed a Preliminary Sur-reply (Paper 9, "PO Sur-reply") directed to the issue of discretionary denial under 35 U.S.C. § 314.

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2016); 37 C.F.R. § 42.4(a) (2019). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an inter partes review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons explained below, we decline to institute an *inter partes* review of the '710 patent.

B. Real Parties in Interest

The parties each identify themselves as the real parties in interest. Pet. 1; Paper 5, 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify the following related matters (Pet. 1–2; Paper 5, 1–2):

Cal. Inst. of Tech. v. Samsung Elecs. Co., No. 2-21-cv-00446 (E.D. Tex. filed Dec. 3, 2021) ("the Underlying Litigation");

Cal. Inst. of Tech. v. Microsoft Corp., No. 6-21-cv-00276 (W.D. Tex. filed Mar. 19, 2021);

Cal. Inst. of Tech. v. HP Inc. f/k/a/ Hewlett-Packard Co., No. 6-20-cv-01041 (W.D. Tex. filed Nov. 11, 2020);

Cal. Inst. of Tech. v. Dell Techs. Inc., No. 6-20-cv-01042 (W.D. Tex. filed Nov. 11, 2020);

Cal. Inst. of Tech. v. Broadcom Ltd., No. 2:16-cv-03714 (C.D. Cal. filed May 26, 2016);

Cal. Inst. of Tech. v. Hughes Commc'ns, Inc., No. 2:15-cv-01108 (C.D. Cal. filed Feb. 17, 2015); and

Cal. Inst. of Tech. v. Hughes Commc'ns, Inc., 2:13-cv-07245 (C.D. Cal. filed Oct. 1, 2013).

The '710 patent was previously the subject of five *inter partes* reviews identified by the parties (Pet. 2; Paper 5, 2–3): IPR2015-00067 ("067 IPR"), IPR2017-00068 ("068 IPR"), IPR2017-00210 ("210 IPR"), IPR2017-00211 ("211 IPR"), and IPR2017-00219 ("219 IPR"). In the Final Written Decisions from the 210 and 219 IPRs, the Board determined that claims 1–8, 10–17, and 19–33 of the '710 patent were not shown to be unpatentable over "Frey," "Divsalar," and "Luby" (for the 210 IPR) and "Divsalar," "Luby," and "Luby97" (for the 219 IPR). None of those references are at issue in this proceeding.

Patent Owner also identifies the following prior *inter partes* review proceedings for patents related to the '710 patent (Paper 5, 2–3): IPR2015-00059, IPR2015-00060, IPR2015-00061, IPR2015-00067, IPR2015-00068, IPR2015-00081, IPR2017-00297, IPR2017-00423,

IPR2017-00700, IPR2017-00701, IPR2017-00702, IPR2017-00703, and IPR2017-00728.

We additionally identify the following co-pending *inter partes* review proceedings between the parties: IPR2023-00131, IPR2023-00133, and IPR2023-00137.

D. The '710 Patent

The '710 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1001, code (54). It explains some of the prior art with reference to its Fig. 1, reproduced below.

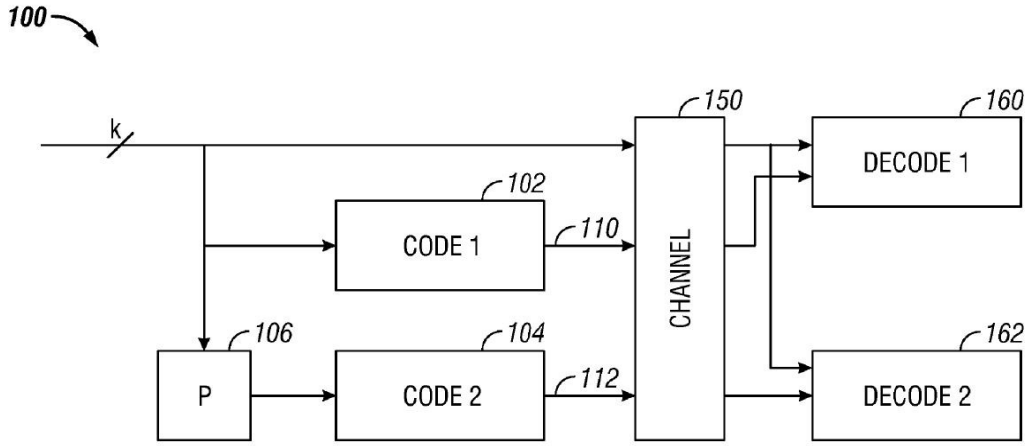

FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:14–15. The '710 patent specification describes Figure 1 as follows:

> A standard turbo coder 100 is shown in FIG. 1. A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102,104 are typically recursive convolutional coders.

> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:38–53 (emphasis omitted).

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

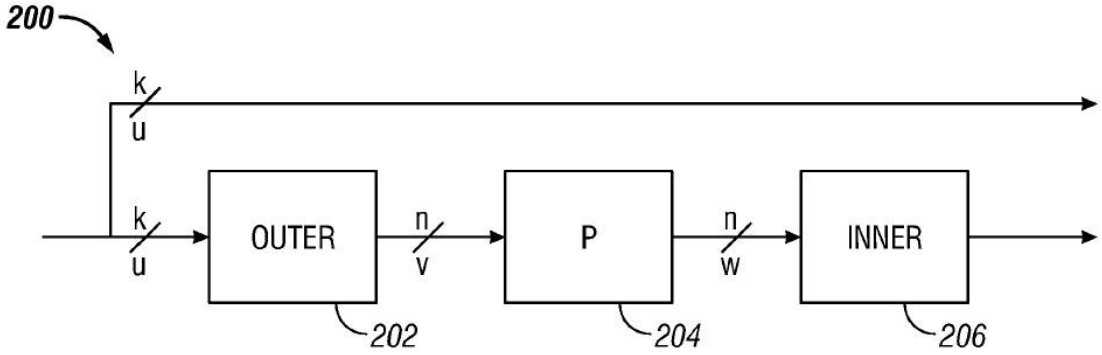

FIG. 2

Figure 2 of the '710 patent is a schematic diagram of coder 200. *Id.* at 2:16–17.

The specification states that "coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206." *Id.* at 2:34–35. It further states as follows:

> The outer coder 202 receives uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship

> between u and v is $v=T_0u$, where T_0 is an n×k matrix, and the rate[1] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence, or degree profile, of the code.
>
> The inner coder 206 may be a linear rate-1 coder, which means that then-bit output block x can be written as $x=T_Iw$, where T_I is a nonsingular n×n matrix. The inner coder 210 can have a rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of 1.

Id. at 2:41–64 (emphasis omitted). Codes characterized by a regular repeat of message bits into a resulting codeword are referred to as "regular repeat," whereas codes characterized by irregular repeat of message bits into a resulting codeword are referred to as "irregular repeat." The second ("inner") encoder 206 performs an "accumulate" function. Thus, the two step encoding process illustrated in Figure 2, including a first encoding ("outer encoding") followed by a second encoding ("inner encoding"), results in either a "regular repeat accumulate" ("RRA") code or an "irregular repeat accumulate ("IRA") code, depending upon whether the repetition in the first encoding is regular or irregular.

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[1] We understand that the "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits.

Figure 4 of the ’710 patent, reproduced below, shows an alternative embodiment in which the first encoding is carried out by a low-density generator matrix.

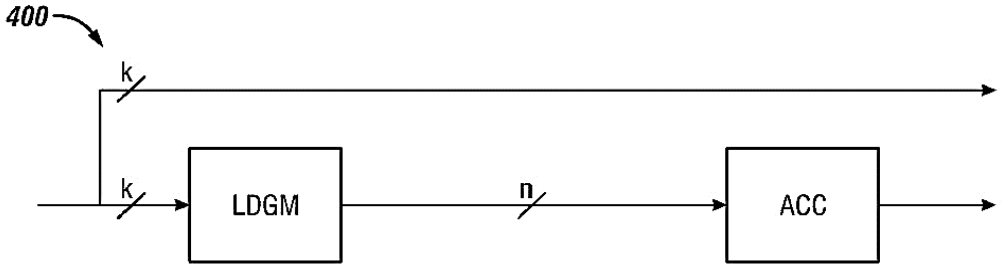

FIG. 4

Figure 4 of the ’710 patent is a schematic of an irregular repeat and accumulate coder using a low-density generator matrix (LDGM)[2] coder. *Id.* at 2:20–21, 3:25. The LDGM coder “performs an irregular repeat of the k bits in the block, as shown in FIG. 4.” *Id.* at 3:52–54. LDGM codes are a special class of low-density parity check codes that allow for less encoding and decoding complexity. LDGM codes are systematic linear codes generated by a “sparse” generator matrix. No interleaver (as in the Figure 2 embodiment) is required in the Figure 4 embodiment because the LDGM provides scrambling otherwise provided by the interleaver.

[2] A “generator” matrix (typically referred to by “G”) is used to create (generate) codewords. A parity check matrix (typically referred to by “H”) is used to decode a received message.

E. Challenged Claims

Claims 11–17 and 19–33 are challenged. Of the challenged claims, claims 11, 15, and 25 are independent.

Claim 11 recites:

> 11. A method of encoding a signal, comprising:
>
> receiving a block of data in the signal to be encoded, the data block including a plurality of bits;
>
> first encoding the data block such that each bit in the data block is repeated and two or more of said plurality of bits are repeated a different number of times in order to form a first encoded data block; and
>
> second encoding the first encoded data block in such a way that bits in the first encoded data block are accumulated.

Ex. 1001, 7:49–59. Claims 12–14 depend from claim 11. *Id.* at 7:60–65.

Independent claim 15 recites:

> 15. A coder comprising:
>
> a first coder having an input configured to receive a stream of bits, said first coder operative to repeat said stream of bits irregularly and scramble the repeated bits; and
>
> a second coder operative to further encode bits output from the first coder at a rate within 10% of one.

Id. at 8:1–7. Challenged claims 16, 17, and 19–24 depend from claim 15. *Id.* at 8:7–15, 8:19–31.

Independent claim 25 recites:

> 25. A coding system comprising:
>
> a first coder having an input configured to receive a stream of bits, said first coder operative to repeat said stream of bits irregularly and scramble the repeated bits;

a second coder operative to further encode bits output from the first coder at a rate within 10% of one in order to form an encoded data stream; and

a decoder operative to receive the encoded data stream and decode the encoded data stream using an iterative decoding technique.

Id. at 8:32–41. Challenged claims 26–33 depend from claim 25. *Id.* at 8:42–63.

F. Prior Art and Asserted Grounds of Unpatentability

Petitioner asserts that claims 11–17 and 19–33 are unpatentable on the following grounds:[3]

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
11, 12, 14–17, 19, 21, 22, 24–27, 29, 32, 33	102(e)	Kobayashi[4]
13, 16, 17, 20, 23, 28	103(a)	Kobayashi
13, 20, 25–33	103(a)	Kobayashi, McEliece[5]

[3] For purposes of this Decision, we assume the claims at issue have an effective filing date not later than March 16, 2013, the effective date of certain amendments in the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), and we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

[4] Kobayashi et al., U.S. Pat. No. 6,029,264, filed Apr. 28, 1997, issued Feb. 22, 2000 (Ex. 1005, "Kobayashi").

[5] McEliece et al., *Turbo Decoding as an Instance of Pearl's "Belief Propagation" Algorithm*, 16 IEEE J. ON SELECTED AREAS IN COMM. 140 (Feb. 1998) (Ex. 1006, "McEliece").

As further support, Petitioner offers the Declaration of Matthew C. Valenti, Ph.D. Ex. 1002.

II. ANALYSIS

A. Principles of Law

A claim is anticipated if a single prior art reference either expressly or inherently discloses every limitation of the claim. *Orion IP, LLC v. Hyundai Motor Am.*, 605 F.3d 967, 975 (Fed. Cir. 2010). Although the elements must be arranged or combined in the same way as in the claim, "the reference need not satisfy an *ipsissimis verbis* test," i.e., identity of terminology is not required. *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009) (citing *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990)).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.[6] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

[6] No evidence of secondary considerations is before us, and, therefore, secondary considerations do not constitute part of our analysis herein.

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

B. Level of Ordinary Skill in the Art

The level of skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham*, 383 U.S. at 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)).

Relying on the declaration testimony of Dr. Valenti, Petitioner asserts a person of ordinary skill in the art of the '710 patent "would have had a Ph.D. in mathematics, electrical or computer engineering, or computer science with an emphasis in signal processing, communications, or coding, or a master's degree in the above areas with at least three years of work experience in the field at the time of the alleged invention." Pet. 5 (citing Ex. 1002 ¶¶ 21–22). Petitioner further states that "[a]dditional education would compensate for less experience, and vice versa." *Id.*

Patent Owner does not offer a different assessment.

To the extent necessary, and for purposes of this Decision, we adopt the definition offered by Petitioner, as it is consistent with the teachings of

the '710 patent and the prior art of record. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (noting that the prior art itself may reflect an appropriate level of skill in the art).

C. Claim Construction

In interpreting the claims of the '710 patent, we "us[e] the same claim construction standard that would be used to construe the claim[s] in a civil action under 35 U.S.C. [§] 282(b)." *See* 37 C.F.R. § 42.100(b) (2022). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as would have been understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc).

Petitioner proposes that the term "repeat," as recited in claims 11, 15, 16, 25, and 26, should be construed to mean "generation of additional bits, where generation can include, for example, duplication or reuse of bits." Pet. 8. As support, Petitioner notes that this construction was adopted by the District Court in *California Institute of Technology v. Broadcom Ltd.*, and affirmed by the Federal Circuit. *California Inst. of Tech v. Broadcom Ltd.*, 25 F.4th 976, 986 (Fed. Cir. 2022).[7] Petitioner states that, in affirming this construction, "the Federal Circuit agreed with the district court and [Patent Owner] that the claims simply require bits to be repeated and do not limit how the duplicate bits are created or stored in memory." Pet. 8. Petitioner also states that "the Federal Circuit found that simply passing an input bit

[7] Subsequent to the parties' main briefing, the District Court in the Underlying Litigation adopted this same construction. Ex. 1019, 21.

through an AND gate (when the other input was '1') was 'repeating' within the context of the asserted claims." *Id.* (citing *Broadcom*, 25 F.4th at 986–88).

Patent Owner does not offer a different construction, nor does Patent Owner dispute this construction. Prelim. Resp. 3. Patent Owner does, however, take issue with Petitioner's application of this construction, asserting that Petitioner is "mischaracterize[ing] the Federal Circuit's construction" and "extend[ing] this construction in an unreasonable way." *Id.* We address Patent Owner's arguments *infra* in connection with our assessment of the strength of Petitioner's showing for purposes of institution.

Consistent with the court in the Underlying Litigation, we adopt the construction of "repeat," as proposed by Petitioner and not disputed by Patent Owner, as meaning "generation of additional bits, where generation can include, for example, duplication or reuse of bits."

We otherwise determine that no other claim term requires express interpretation at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Discretionary Denial Under 35 U.S.C. § 314

In view of co-pending district court litigation, our disposition of this case turns on the issue of discretionary denial. Patent Owner contends we should exercise our discretion to deny institution under 35 U.S.C. § 314(a). Prelim. Resp. 36–50; PO Sur-reply 1–3. Petitioner contends that we should not deny institution based on discretionary factors. Pet. 63–71; Pet. Reply 1–3.

Institution of *inter partes* review is discretionary. *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) ("[Section] 314(a) invests the Director with discretion on the question whether to institute review . . . ." (emphasis omitted); *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016) ("[T]he agency's decision to deny a petition is a matter committed to the Patent Office's discretion."); *Harmonic*, 815 F.3d at 1367 ("[T]he [Office] is permitted, but never compelled, to institute an [*inter partes* review] proceeding.").

In *Apple Inc. v. Fintiv Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"), the Board discussed potential applications of *NHK Spring Co., Ltd. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential) ("*NHK*"), as well as a number of other cases dealing with discretionary denial under § 314(a). *Fintiv* identifies a non-exclusive list of factors parties may consider addressing, particularly where there is a related, parallel district court action and whether such action provides any basis for discretionary denial. *Fintiv*, Paper 11 at 5–16. Those factors include:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;

3. investment in the parallel proceeding by the court and the parties;

4. overlap between issues raised in the petition and in the parallel proceeding;

5. whether the petitioner and the defendant in the parallel proceeding are the same party; and

6. other circumstances that impact the Board's exercise of discretion, including the merits.

Id. at 5–6.

Our analysis of the *Fintiv* factors is guided by the USPTO Director's Memorandum issued on June 21, 2022, titled "Interim Procedure for Discretionary Denials in AIA Post Grant Proceedings with Parallel District Court Litigation" ("Interim Procedure")[8], which provides several clarifications to the application of the *Fintiv* factors when there is parallel litigation. Interim Procedure 2; *see also CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 (PTAB Feb. 27, 2023) (precedential) ("*CommScope*") (holding that the Board should engage in the compelling merits question only if *Fintiv* factors 1–5 favor discretionary denial).

We now consider these factors to determine whether we should use our discretion to deny institution under 35 U.S.C. § 314(a). In evaluating the factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Fintiv*, Paper 11 at 6.

1. Stay in the Underlying Litigation

Under the first *Fintiv* factor, we consider "whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted." *Id.* at 6. Patent Owner notes that Petitioner has already filed a motion for a stay, and the district court denied the motion. Prelim. Resp. 39–40 (citing

[8] *Available at* https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

Ex. 2002, 4–5; Ex. 2003). Petitioner argues that it is not precluded from filing another motion for a stay if we were to institute *inter partes* review. Pet. Reply 2–3.

The district court has already denied a motion for a stay, and the reasoning in its decision on the motion indicates that the court is unlikely to grant a renewed motion. *See* Ex. 2002, 5–6 (finding that the advanced stage of the underlying litigation disfavors a stay and that a stay is unlikely to simplify the issues in the underlying litigation). Thus, we find that this factor weighs in favor of exercising authority to deny institution. *See Fintiv*, Paper 11 at 6–7.

2. The Trial Date in the Underlying Litigation

Under the second *Fintiv* factor, we consider the "proximity of the court's trial date to the Board's projected statutory deadline for a final written decision." *Fintiv*, Paper 11 at 6. Trial in the Underlying Litigation is set to start on September 11, 2023. Pet. 65 (citing Ex. 1015, 1); Prelim. Resp. 41. Petitioner also notes that, under the time-to-trial statistics for the district in which the Underlying Litigation is pending, the trial would be expected to start on December 17, 2023. Pet. 65 (citing Ex. 1016, 35). Our anticipated one-year statutory deadline for issuing a final written decision in this case would be in May 2024.

Regardless of whether we consider the scheduled trial date or the trial date expected based on time-to-trial statistics, the trial in the Underlying Litigation would commence several months before the expected date of our final written decision. Thus, we find that the second *Fintiv* factor favors exercising authority to deny institution.

3. Investment by the Court and the Parties in the Underlying Litigation

Under the third *Fintiv* factor, we consider the "investment in the parallel proceeding by the court and the parties" as of the time of the institution decision. *Fintiv*, Paper 11 at 6, 9–10. Both parties acknowledge that the court in the Underlying Litigation has already issued a claim construction order. Pet. Reply 1; PO Sur-reply 2; *see also* Ex. 1019 (order). In addition, Patent Owner contends that "[b]y the expected May institution decision date, substantial pretrial work related to validity will be complete: fact discovery will be closed, expert reports will be served, and all dispositive motions will be due within a month." PO Sur-reply 1 (citing Ex. 1015, 3).

Although Petitioner disputes the significance of claim construction to our consideration of this factor (*see* Pet. Reply 1), we find that the advanced stage of expert discovery is the most significant fact for our analysis.[9] In particular, the scheduling order in the Underlying Litigation indicates that Petitioner should have already served its opening expert report on validity. Ex. 1015, 3. Given that the deadline for rebuttal expert reports is only days away (*see id.*), we also can safely assume that work pertaining to a rebuttal expert report on validity is well underway. We consider this work

[9] As noted *supra* Section II.C., the Petition, for the term "repeat," relies on a construction made by the District Court for the Central District of California in an earlier proceeding (and affirmed by the Federal Circuit). Pet. 8–9 (citing *Cal. Inst. of Tech. v. Broadcom Ltd.*, 25 F.4th 976, 986 (Fed. Cir. 2022)). This construction was also discussed by the parties, and adopted by the District Court, in the Underlying Litigation. *See* Ex. 1019, 19–21. This indicates that there has been investment by multiple courts, including the court in the Underlying Litigation, that is pertinent to patentability issues before us. *See* Prelim. Resp. 43; PO Sur-reply 2.

significant because it relates directly to the merits of the parties' invalidity positions. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 10–11 (PTAB June 16, 2020) (informative) ("*Sand Revolution*").

As part of this factor, we additionally consider whether Petitioner unreasonably delayed in filing the Petition in this case. *See Fintiv*, Paper 11 at 11–12. Patent Owner argues that Petitioner waited approximately 10 months after Patent Owner filed the Underlying Litigation before Petitioner filed the instant Petition.[10] Prelim. Resp. 44. Petitioner argues that it filed the Petition "just seven months after being served with preliminary infringement contentions . . . , which identified the asserted claims." Pet. 67. Petitioner asserts this timing was reasonable given that Patent Owner "asserted four patents containing over 90 issued claims." *Id.* Although Petitioner did file its Petition somewhat late in the statutory period and some months after receiving infringement contentions, we do not view this timing to be as significant as the advanced stage of case development in the Underlying Litigation regarding invalidity.

Accordingly, on the whole, this factor weighs in favor of exercising our authority to deny institution.

[10] We acknowledge that the timeliness of a petition is measured from the date on which a complaint alleging patent infringement is served. *See* 35 U.S.C. § 315(b). In the Underlying Litigation, Petitioner waived the service requirement 17 days after the complaint was filed. *See* Underlying Litigation, ECF No. 9. The 17-day difference between filing and waiver of service does not impact our analysis.

4. Overlap of the Issues

Under the fourth *Fintiv* factor, we consider the "overlap between issues raised in the petition and in the parallel proceeding." *Fintiv*, Paper 11 at 6. Petitioner stipulates that, if we were to institute *inter partes* review, it would not "pursue invalidity challenges to the '710 Patent in the parallel district court lawsuit that rely on any reference used in the grounds of the Petition (Kobayashi and McEliece)." Pet. Reply 1. Patent Owner argues that Petitioner can still put forth district court invalidity arguments based on references that are "integral to" the asserted grounds, including "Lin/Costello and MacKay." PO Sur-reply 1; *see also* Prelim. Resp. 46 (similar argument).

Petitioner's stipulation is not as expansive as the stipulation discussed in *Sotera Wireless Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 13 (PTAB Dec. 1, 2020) (precedential) ("*Sotera*"), because Petitioner does not relinquish all grounds that it reasonably could have raised in this *inter partes* review.[11] Nevertheless, it is broader to some degree than the stipulation discussed in *Sand Revolution* because it precludes Petitioner from relying in the district court on any of the same references listed in the statement of the grounds in the Petition, and is not limited to only the same grounds. *See Sand Revolution*, Paper 24 at 11–12. We find that Petitioner's stipulation mitigates some concerns of duplicative efforts between the district court and the Board. Notwithstanding, the fact that Petitioner's arguments also rely on non-grounds references "Lin/Costello and MacKay," which are not subject

[11] As such, Petitioner does not qualify for the treatment described in the Interim Procedure for *Sotera* stipulations. *See* Interim Procedure at 7–8.

to Petitioner's stipulation, diminishes the impact of Petitioner's stipulation to some extent.

Accordingly, we find that this factor weighs somewhat against exercising our discretion to deny institution.

5. Whether Petitioner is Unrelated to the Defendant in the Underlying Litigation

Under the fifth *Fintiv* factor, we consider "whether the petitioner and the defendant in the parallel proceeding are the same party." *Fintiv*, Paper 11 at 6. We determine that the fifth *Fintiv* factor favors exercising our discretion to deny institution because Petitioner, Samsung Electronics Co., Ltd., is a defendant in the Underlying Litigation. *See* Prelim. Resp. 47; *Sotera*, Paper 12 at 19.

6. Summary Regarding Fintiv Factors 1–5

In summary, factors 1–3 and 5 weigh in favor of exercising our discretion to deny institution and factor 4 weighs somewhat against exercising our discretion to deny institution. Considering these factors as a whole, we determine that these factors weigh in favor of exercising our discretion to deny institution.

7. Other Circumstances Including the Merits

Under the sixth *Fintiv* factor, we consider "other circumstances that impact the Board's exercise of discretion, including the merits." *Fintiv*, Paper 11 at 6.

First, we turn to the merits of the Petition. Because we conclude that *Fintiv* factors 1–5 in this proceeding favor discretionary denial, we consider whether the Petition presents a challenge with compelling merits. Interim Procedure 4–5. That is, we consider whether the challenges' "evidence, if

unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence." *Id.* at 4. "A challenge can only 'plainly lead to a conclusion that one or more claims are unpatentable' if it is highly likely that the petitioner would prevail with respect to at least one challenged claim." *OpenSky Indus., LLC v. VLSI Tech. LLC*, IPR2021-01064, Paper 102 at 49 (PTAB Oct. 4, 2022) (precedential) (quoting Interim Procedure at 4). The "compelling merits" standard is a standard higher than that required for institution. *CommScope*, Paper 23 at 3.

For the reasons given below (*infra* Section II.E.), we determine that Petitioner has not presented a compelling, meritorious challenge to the claims of the '710 patent. Thus, this consideration is neutral as to whether we should exercise our discretion to deny the Petition.

As another consideration for the sixth *Fintiv* factor, Patent Owner asks us to consider the history of *inter partes* reviews against the '710 patent and its related patents. PO Sur-reply 48–50; *see supra* I.C. (related matters). In particular, Patent Owner argues that "this is the sixth IPR against the '710 patent, and none of the prior five found even a single claim unpatentable." Prelim. Resp. 48. Patent Owner further argues that "the Board has already invested substantial resources reviewing repeated IPR challenges and repeatedly upholding the claims of the '710 patent and its family members." *Id.* at 49. Petitioner downplays the relevance of the prior *inter partes* reviews because they were mostly based on "obviousness combinations, some up to *four* references," whereas one ground in this case relies on a single reference. Pet. Reply 3. Petitioner also characterizes the multiple prior *inter partes* reviews as a consequence of Patent Owner's "own choice

to litigate its claims serially." *Id.* In consideration of the Board's prior expenditure of resources reviewing the claims of the '710 patent, and in light of the outcomes of these prior reviews, we view the prior unsuccessful challenges against the challenged claims as slightly favoring discretionary denial.

Thus, on the whole, we find the sixth *Fintiv* factor to weigh slightly in favor of exercising our discretion to deny institution.

8. Conclusion

Petitioner's stipulation is the only circumstance that weighs against discretionary denial. We find that the advanced posture of the Underlying Litigation outweighs the impact of Petitioner's stipulation. In particular, trial is set to start approximately eight months before the expected date of our final written decision. The parties also have engaged in relevant case development in the Underlying Litigation insofar as expert discovery on validity is well underway. Moreover, the court in the Underlying Litigation has already denied Petitioner's bid for a stay in that case. Thus, based on our holistic view of the *Fintiv* factors, we exercise our discretion under 35 U.S.C. § 314(a) to deny the Petition.

E. Merits Analysis

1. Overview of Kobayashi (Ex. 1005)

Kobayashi is a United States patent titled "System and Method for Error Correcting a Received Data Stream in a Concatenated System." Ex. 1005, code (54). Kobayashi issued on February 22, 2000, based on an application filed on April 28, 1997. *Id.* at codes (43), (22). Petitioner asserts that Kobayashi is prior art under 35 U.S.C. §§ 102(a), 102(e). Pet. 4. Patent Owner does not dispute the prior-art status of Kobayashi

Kobayashi discloses a concatenated encoding and decoding system with transmitter and receiver portions, shown at the top and bottom, respectively, of Figure 8, reproduced below.

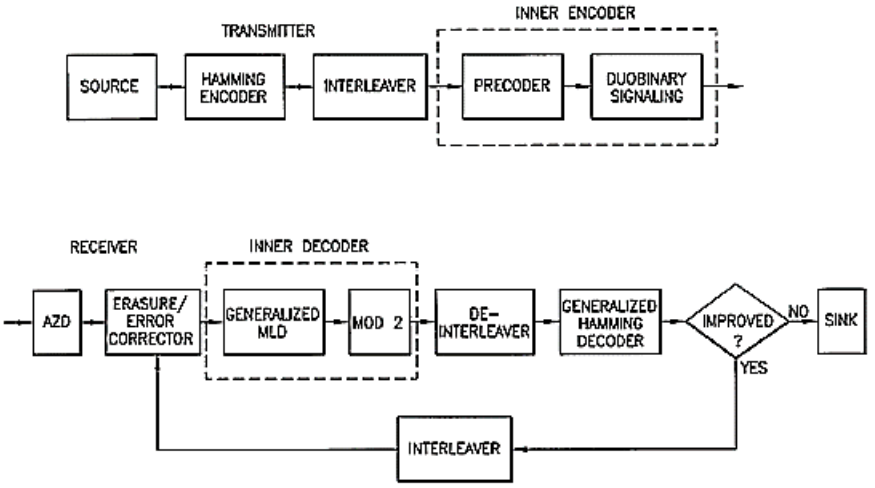

FIG.8

Figure 8 of Kobayashi is a block diagram depicting a concatenated system incorporating "a Hamming code and duobinary signalling." Ex. 1005, 5:25–27.

Kobayashi's transmitter is for "a simple packet transmission system in which there are 28 information bits in a packet," and which is designated I_1. *Id.* at 7:46–49. After obtaining the 28 information bits for transmission, Kobayashi's transmitter then performs several encoding steps, first segmenting the packet into seven 4-bit blocks, and then encoding each block to generate a corresponding 7–bit block using a (7,4) Hamming code, resulting in 49 total bits, the sequence of which is designated as I_2. *Id.* at 7:50–65. Next, the transmitter "perform[s] a permutation action" using a 7x7 interleaver that stores the 49 bits in an array structure, reading the data in row-wise and outputting the data column-wise. *Id.* at 8:3–20. "The precoder output is obtained by taking the modulo-2 sum of the current input

and the previous output." *Id.* at 8:21–27. A duobinary sequence is observed at the channel output. *Id.* at 8:28–32.

Kobayashi's receiver receives a duobinary sequence, passes it through an ambiguity zone detector (AZD), and begins an iterative decoding method that "attempts to resolve as many erasures/errors as possible" on each iteration. *Id.* at 8:33–67.

2. Analysis

As discussed *supra* Section II.D., we have determined that discretionary denial is appropriate under the circumstances of this proceeding unless Petitioner's showing on the merits rises to the level of "compelling"—that is, unless Petitioner has demonstrated that it is highly likely to prevail with respect to at least one challenged claim. *See OpenSky* IPR2021-01064, Paper 102 at 49 (quoting Interim Procedure at 4).

We have reviewed the arguments and evidence presented. For our purposes here, we assume that Petitioner makes a sufficient showing to establish that Kobayashi discloses certain limitations of the challenged claims, including generally disclosing "encoding a signal" and "receiving a block of data in the signal to be encoded," as recited in independent claim 11 and similarly recited in independent claims 15 and 25. For the reasons discussed below, however, we do not find compelling Petitioner's showing for at least the step of "first encoding the data block such that each bit in the data block is repeated and *two or more of said plurality of bits are repeated a different number of times* in order to form a first encoded data block," as recited in claim 11, and a first coder "operative to *repeat said stream of bits irregularly* and scramble the repeated bits," as recited in claims 15 and 25.

Central to Petitioner's argument regarding this limitation is the following syllogism: (1) "the Federal Circuit found that passing an input information bit through an AND gate when the other input is a '1' bit comprises 'repeating' the information bit"; and (2) "multiplying a binary information bit by a '1' bit is equivalent to passing the information bit through an AND gate with a '1' bit"; therefore, (3) "multiplying an information bit by a '1' bit comprises 'repeating' the information bit." Pet. 14–15 (citing Ex. 1002 ¶ 64; Ex. 1009, 7–8). Petitioner extrapolates that "under this construction, any type of linear code using a non-zero generator matrix will 'repeat' input bits because the process of multiplying a vector of information bits by the generator matrix will necessarily involve multiplying input bits by '1' bits." *Id.* at 15 (citing Ex. 1002 ¶ 64).

Petitioner then argues that Kobayashi's Hamming encoder creates the 49-bit "'first encoded data block' I_3" by "multiplying each 4-bit sub-block of I_1 by the 4x7 generator matrix G, resulting in seven 7-bit codewords," and then "[t]he interleaving operation permutes the order of these bits." Pet. 15 (citing Ex. 1002 ¶ 65). Petitioner asserts:

> This "first encoding" step performs *repetition* of each and every information bit because the process of multiplying each 4-bit sub-block by generator matrix G involves multiplying each input bit by at least one "1" bit (i.e., repeating the input bits) and then summing the repeated bits to generate the codeword. . . . Moreover, the information bits are repeated irregularly such that information bits are repeated a different number of times.

Id. (citations omitted) (citing Ex. 1002 ¶¶ 65, 66).

Patent Owner counters by challenging the core premise of Petitioner's argument:

> Petitioner misinterprets the Federal Circuit's construction of "repeat," stretching the actual construction to conclude that every act of "multiplying a bit by a '1' bit comprises 'repeating' the information bit," on the basis that passing a bit through an AND gate can perform an operation "equivalent" to multiplying by "1." Pet., 14-15. Petitioner then further extends this interpretation, arguing that if an encoder, such as Kobayashi's Hamming encoder, performs a transform that can be characterized by a non-zero generator matrix with different numbers of "1"s in different rows, then that encoder must necessarily repeat bits different numbers of times or irregularly. *See* Pet., 15-16. Petitioner does not justify its logical leap from a finding of infringement by a particular device that duplicated bits and sent them through a specific configuration of AND gates to a conclusion that every implementation of a transformation that could be performed using binary multiplication must repeat bits.

Prelim. Resp. 11.

For essentially the reasons posed by Patent Owner, we agree that Petitioner's showing is less than compelling, as it rests tenuously upon apparent logical leaps. First, the Federal Circuit's holding in *Broadcom* does not support Petitioner's inference that every act of multiplying a bit by "1" comprises repeating that bit. In *Broadcom*, the Federal Circuit found that the jury's verdict of infringement of the '710 patent was supported by "substantial evidence" in the form of expert testimony that the accused devices allowed information bits to "flow through" to an output gate when the information bit was input to an AND gate with a parity-check bit of 1. *Broadcom*, 25 F.4th at 987. The expert also testified that the number of information bits that were allowed to flow through varied, resulting in

irregular repetition. *Id.* at 987–88. The Federal Circuit determined that, in light of this testimony, "[w]e are not persuaded that the record before the jury permits only a verdict of no infringement." *Id.* at 988.

In the case before us, as Patent Owner points out, Petitioner does not justify its logical leap from a finding of infringement by a particular device that duplicated bits by passing them through a specific configuration of AND gates, as in *Broadcom*, to a conclusion that every implementation of a transformation that could be performed using binary multiplication must repeat bits. In *Broadcom*, the expert testimony emphasized that certain bits were "repeated" because they were allowed to "flow through" an AND gate to an output gate. *Broadcom*, 25 F.4th at 987. Petitioner's showing here is different—it is premised on multiplying certain data bits by 1 as an intermediate step in matrix multiplication. *See* Pet. 15–16 (purporting to depict Kobayashi's generation of data block I_3). Petitioner's general assertion that "[m]ultiplying a binary information bit by a '1' bit is equivalent to passing the information bit through an AND gate with a '1' bit" (*id.* at 14–15) does not fully account for the differences in these operations—information bits flowing through an AND gate to an output gate, as in *Broadcom*, versus information bits being subjected to matrix multiplication to generate an expanded data block, as here. Even if we were to deem Petitioner's gap in reasoning surmountable for a showing of a reasonable likelihood of success (a finding we do not make), we apply a higher compelling merits standard for purposes of determining whether to exercise our discretion to deny institution. Because of the gap, Petitioner has not made an adequate showing under that higher standard.

Patent Owner provides additional arguments that undermine the strength of Petitioner's showing. In particular, Patent Owner asserts that "even assuming that multiplying bits by '1' constitutes repetition . . . , Kobayashi never discloses any such multiplication for its outer encoder." Prelim. Resp. 13. Rather, as Patent Owner also asserts, although "Kobayashi describes the inputs to its encoder and how the encoder's output is mathematically related to its inputs, it provides almost no details as to what process its outer encoder uses to generate its outputs." *Id.* Thus, according to Patent Owner, "Kobayashi also never describes its outer encoder as multiplying input bits by anything." *Id.* Patent Owner concludes:

> While Kobayashi specifies the result of its encoding (namely, that the output of its encoder is related to the input by the specified generator and parity-check matrices), it never provides any details of how the output is actually computed. In particular, Kobayashi never states that the bits input to the Hamming encoder are repeated in any way, much less irregularly. Nor does Kobayashi say that the input bits are multiplied by "1"s at all, and certainly not different numbers of times.

Id. at 14; *see also id.* at 15–19 (arguing that Petitioner also has not shown that Kobayashi *inherently* discloses irregular repetition by multiplying different input bits by "1" different numbers of times). Patent Owner also asserts that, although Kobayashi does not describe how the outer encoder operates, it does provide details regarding the precoder, which, according to Petitioner, also performs a linear transform with a non-zero generator matrix that has different numbers of "1"s in different rows. *Id.* at 20–22. In particular, Kobayashi states that the "precoder output is obtained by taking the modulo-2 sum of the current input and the previous input," which Patent

Owner states is not a multiplication. *See id*. at 22 (citing Ex. 1005, 8:21–24, 3:15–16). Patent Owner concludes:

> Thus, contrary to the petition's assumptions regarding linear transforms, Petitioner's own description of Kobayashi's precoder implies that a component of an encoder may perform a linear transform that can be characterized by a non-zero generator matrix with different numbers of "1"s in each column, yet neither multiply input bits nor irregularly repeat them.

Id.

We agree that Kobayashi provides scant details on the operation of its outer encoder, which Petitioner attempts to fill in with expert testimony on Hamming coders and matrix multiplication generally. *See* Ex. 1002 ¶¶ 28–35, 64. Patent Owner, on the other hand, provides argument based on Kobayashi's disclosure and Petitioner's own characterization of that disclosure that appears, on this record, to contradict Petitioner's arguments. Even if, hypothetically, we were to deem Petitioner's showing on the record before us to be adequate under the lesser reasonable likelihood standard (again, a finding we do not make), we apply a higher compelling merits standard for our analysis of the sixth *Fintiv* factor, and find Petitioner has not met that higher standard.

In short, on the record before us, for the reasons noted above, we do not view Petitioner's evidence as plainly leading to a conclusion that one or more claims are unpatentable by a preponderance of the evidence. *See* Interim Procedure 4. We, therefore, find Petitioner's showing as to the independent claims is not compelling.

Petitioner's arguments for the dependent claims and the other grounds (including the ground based on the combination with McEliece) (Pet. 19–56)

do not cure the above deficiencies. Thus, Petitioner's showing of unpatentability is not compelling for any of the challenged claims under any of the asserted grounds.

III. CONCLUSION

For the reasons above, we exercise our discretion under 35 U.S.C. § 314(a) to deny institution of *inter partes* review.

IV. ORDER

Accordingly, it is

ORDERED that the Petition is denied as to all challenged claims, and no *inter partes* review is instituted.

PETITIONER:

Robert A. Appleby
Greg S. Arovas
KIRKLAND & ELLIS, LLP
robert.appleby@kirkland.com
greg.arovas@kirkland.com

PATENT OWNER:

Michael T. Rosato
Matthew A. Argenti
Patrick M. Medley
WILSON SONSINI GOODRICH & ROSATI
mrosato@wsgr.com
margenti@wsgr.com
pmedley@wsgr.com