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Paper 14
Entered: July 6, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,
Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,
Patent Owner.

IPR2022-00309
Patent 8,035,112 B1

Before GRACE KARAFFA OBERMANN, JO-ANNE M. KOKOSKI, and JEFFREY W. ABRAHAM, *Administrative Patent Judges.*

KOKOSKI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

STMicroelectronics, Inc. ("Petitioner") filed a Petition to institute an *inter partes* review of claims 1, 6, 7, and 10–12 (the "challenged claims") of U.S. Patent No. 8,035,112 B1 ("the '112 patent," Ex. 1001). Paper 2 ("Pet."). The Trustees of Purdue University ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp.").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2021). Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the '112 patent, and we decline to exercise our discretion to deny institution under 35 U.S.C. §§ 314(a) or 325(b). Accordingly, for the reasons that follow, we institute an *inter partes* review of claims 1, 6, 7, and 10–12 of the '112 patent.

A. Real Parties in Interest

Petitioner identifies STMicroelectronics, Inc., STMicroelectronics N.S., and STMicroelectronics International N.V. as the real parties in interest. Pet. 1. Patent Owner identifies The Trustees of Purdue University and the Purdue Research Foundation as the real parties in interest. Paper 7, 1.

B. Related Matters

The parties indicate that the '112 patent is asserted in *The Trustees of Purdue University v. STMicroelectronics N.V*, No. 6:21-CV-00727 (W.D.

Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). Pet. 1–2; Paper 11, 1. Patent Owner also identifies *STMicroelectronics, Inc. v The Trustees of Purdue University*, IPR2022-00724 (filed on March 25, 2022), and *Wolfspeed, Inc. v. The Trustees of Purdue University*, IPR2022-00854 (filed on April 12, 2022) as related matters. Paper 11, 1.

C. The '112 Patent

The '112 patent relates to a high voltage power metal oxide field effect transistor ("MOSFET") that includes a silicon carbide ("SiC") wafer having a substrate, a drift layer, a plurality of source regions, a first oxide layer, a plurality of polysilicon gates, and a second oxide layer of greater thickness than the first oxide layer. Ex. 1001, 2:27–37.

The '112 patent explains that "[p]ower MOSFETs are well known for their ability to carry large currents in the on-state while withstanding large breakdown voltages in the off-state." Ex. 1001, 1:26–28. In MOSFET devices, current flow between the source and drain regions in a semiconductor substrate is controlled by a voltage applied to a gate electrode, which is separated from the semiconductor surface by an insulator such as silicon dioxide. *Id*. at 1:28–31. "Lateral and vertical power MOSFET structures in silicon have been explored over the years, the former type having the drain, gate and source terminals on the same surface of the silicon wafer, the later type having the source and drain on opposite surfaces of the wafer." *Id*. at 1:38–42. "Several different types of vertical power MOSFETs have been proposed, including the double-diffused MOSFET ("DMOSFET") and the trench-gate or UMOSFET." *Id*. at 1:42–45.

According to the '112 patent, an important performance parameter in power DMOSFETs is the specific on-resistance, which is defined as the

product of the resistance when the device in the on, or highly conducting, state, multiplied by the area of the device. Ex. 1001, 1:61–65. Therefore, "it is important to minimize both the resistance and the area of the device." *Id*. at 1:65–66. The '112 patent teaches that "a significant component of the total resistance is the resistance of the source contacts." *Id*. at 2:1–2. Although larger-area source contacts have lower resistance, increasing the contact area increases the total area of the device, and, as a result, the on-resistance. *Id*. at 2:2–5. Therefore, the '112 patent states that "[i]t is important to find ways to reduce to source contact resistance without increasing the area of the device." *Id*. at 2:5–6.

The '112 patent also teaches that in a conventional DMOSFET, because the source contact is defined by photolithography, "the source contact must be separated from the edge of the gate by sufficient distance so that the source contact and the gate cannot touch even under the worst case misalignment of the source contact mask." Ex. 1001, 2:7–11. Moreover, the actual functional area of the source contact is determined by the overlap of the source contact metal and the N+ implant that forms the source region in the semiconductor. *Id*. at 2:11–14. Because the N+ implant is defined by a separate mask, "relative misalignment of the source contact mask and the N+ implant mask can reduce the functional area of the source contact, thereby increasing the source resistance and degrading performance." *Id*. at 2:14–18. As a result, the '112 patent seeks to "produce DMOSFETs and related devices wherein misalignments of source contact and gate are reduced and eliminated." *Id*. at 2:19–21.

The '112 patent addresses these problems by providing high voltage power MOSFETs with self-aligned source contacts. Ex. 1001, 2:24–26. Figure 3 of the '112 patent is reproduced below.

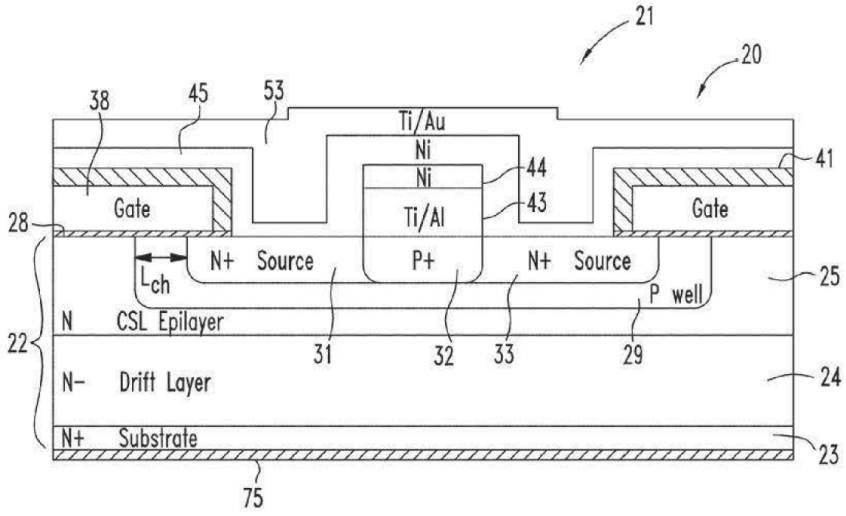


FIG. 3

Figure 3 is a side, cross-sectional view of one cell region of a DMOSFET described in the '112 patent. Ex. 1001, 2:49–50. Cell region 20 of DMOSFET 21 includes substrate 23 and a number of semiconductor layers and implants formed on or in substrate 23 up through top surface 28, which are collectively referred to as substrate body 22. *Id*. at 4:8–11. Formed atop substrate 23, which is heavily doped with N-type impurities to an N+ concentration, is drift layer 24 that is lightly doped to an N- concentration. *Id*. at 4:22–25. On top of drift layer 25 is current spreading epilayer ("CSL") 25 that is "more heavily doped than drift layer 24, but not as heavily doped as substrate 23." *Id*. at 4:25–28. P well 29 is formed in the top of CSL 25, with "two heavily doped N+ implant source regions 31 and 32 on opposing sides of a heavily doped, central implant P+ base 33" formed therein. *Id*. at 4:30–31, 4:51–53. The upper surfaces of P+ base 33, source regions 31 and 32, P well 29, and CSL 25 "are coplanar and together form an upper surface 28 of substrate body 22." *Id*. at 4:59–63.

Formed atop upper surface 28 and centered over the left and right ends of P well 29 "is a polycrystalline (polysilicon) gate 38 that is

surrounded along its top, bottom, left and right sides by an insulating layer of silicon dioxide 41." Ex. 1001, 4:66–5:3. Ti/Al contact metal 43 is formed atop P+ base 33, Ni contact metal 44 is formed atop Ti/Al contact metal 43, and Ni ohmic contact metal 45 is formed over the entirety of MOSFET 21, "overlapping the polysilicon gate 38, but insulated from it by the thick oxide layer 41 on the top and sides thereof." *Id*. at 5:4–8.

The '112 patent teaches that, because polysilicon gate 38 is completely surrounded by insulating oxide layer 41, its position "relative to source contacts 31 and 32 is much less critical, and it cannot detrimentally come into contact with any portion of the Ni metal contact 45 due to any mask misalignment during processing." Ex. 1001, 5:9–13. Additionally, the deposition of Ni metal contact 45 over the entire MOSFET 21 "makes conformal, direct and self-aligning contacts with the Ti/Al and Ni metals 43 and 44 and, most importantly, with N-source implants 31 and 32." *Id*. at 5:19–25.

D. Challenged Claims

Petitioner challenges claims 1, 6, 7, and 10–12 of the '112 patent. Claims 1 and 6 are the only independent claims challenged; claim 1 is illustrative of the claimed subject matter and is reproduced below.

> 1. A silicon carbide power MOSFET, comprising:
>
> a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof;
>
> a plurality of polysilicon gates above said drift layer, said plurality of polysilicon gates including a first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region;
>
> a first oxide layer between said first gate lower surface and said upper surface of said drift layer;

> a second, thicker oxide layer over said top surface and sidewall of said first gate; and
>
> a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region.

Ex. 1001, 8:23–39.

E. Prior Art and Asserted Grounds

Petitioner asserts that claims 1, 6, 7, and 10–12 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 6, 7, 10, 12	103[1]	Ueno[2]
11	103	Ueno, Lidow[3]

Pet. 3–4. Petitioner relies on the Declaration of Vivek Subramanian, Ph.D. (Ex. 1002) in support of its contentions.

II. ANALYSIS

A. 35 U.S.C. § 314(a)

Under 35 U.S.C. § 314(a), the Director has discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) ("[T]he agency's decision to deny a petition is a matter committed to the Patent Office's discretion."); *SAS Inst. v Iancu*, 138 S. Ct. 1348, 1356 (2018) ("[Section] 314(a) invests the Director with discretion on the question *whether* to institute review."); *Harmonic v. Avid*

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the '112 patent has an effective filing date before March 16, 2013 (Ex. 1001, codes (22), (60)), we refer to the pre-AIA version of Section 103.
[2] Ueno, US 6,238,980 B1, issued May 29, 2001 (Ex. 1003).
[3] Lidow, US 4,593,302, issued June 3, 1986 (Ex. 1014).

Tech., Inc., 815 F.3d 1356, 1367 (Fed. Cir. 2016) ("[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.").

In determining whether to exercise discretion to deny institution under 35 U.S.C. § 314(a), the Board considers the trial date in related litigation as part of an assessment of all relevant circumstances of the case, including the merits, in an effort to balance considerations such as system efficiency, fairness, and patent quality. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv* Order"); *see also NHK Spring Co. v. Intri-Plex Techs., Inc*., IPR2018-00752, Paper 8 at 19–20 (PTAB Sept. 12, 2018) (precedential) (denying institution relying, in part, on § 314(a) because the parallel district court proceeding was scheduled to finish before the Board reached a final decision). In particular, the Board evaluates the following factors ("*Fintiv* factors"):

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv Order, 5–6. In evaluating these factors, "the Board takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Id.* at 6.

On June 21, 2022, the Director of the United States Patent and Trademark Office ("USPTO") issued a Memorandum[4] to clarify "the PTAB's current application of *Fintiv* to discretionary institutions when there is parallel litigation" and "confirm[] that the precedential import of *Fintiv* is limited to the facts of that case." Memorandum, 2. In particular, the Memorandum sets forth that: (1) the PTAB will not rely on the *Fintiv* factors to discretionarily deny institution "where a petition presents compelling evidence of unpatentability" (*id*. at 2); (2) the *Fintiv* factors do not apply to parallel U.S. International Trade Commission proceedings (*id*. at 2–3); (3) the PTAB will not discretionarily deny institution "where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB" (*id*. at 3); and (4) "the PTAB will consider the median time from filing to disposition of the civil trial for the district in which the parallel litigation resides" (*id*.).

Patent Owner argues that we should exercise our discretion under 35 U.S.C. § 314(a) to deny institution because of the "accelerated schedule of the parallel pending litigation." Prelim. Resp. 17–24. We have considered the circumstances and facts before us in view of the *Fintiv* factors and the Memorandum, and determine that the information presented in the Petition presents a compelling unpatentability challenge.

The Memorandum explains that "where the PTAB determines that the information presented at the institution stage presents a compelling unpatentability challenge, that determination alone demonstrates that the

[4] Available at: https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

PTAB should not discretionarily deny institution under *Fintiv*." Memorandum, 4–5. "Compelling, meritorious challenges are those in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence." *Id*. at 4. On the current record, we determine that Petitioner's obviousness ground based on Ueno, if unrebutted at trial,[5] would plainly lead to a conclusion that claims 1, 6, 7, 10, and 12 are unpatentable by a preponderance of the evidence. *See infra* Section II.E. Instituting *inter partes* review under these circumstances "strikes a balance among the competing concerns of avoiding potentially conflicting outcomes, avoiding overburdening patent owners, and strengthening the patent system by eliminating patents that are not robust and reliable." Memorandum, 5; *see also Fintiv* Order, 14–15 (When the merits of a ground raised in the petition seem particularly strong on the preliminary record, "the institution of trial may serve the interest of overall system efficiency and integrity because it allows the proceeding to continue in the event that the parallel proceedings settles or fails to resolve the patentability questions presented in the PTAB proceeding.").

Accordingly, we decline to exercise our discretion under § 314(a) to deny institution of *inter partes* review.

B. 35 U.S.C. § 325(d)

Patent Owner argues that we should exercise our discretion under 35 U.S.C. § 325(d) to deny institution because Ueno was previously considered during the prosecution of the '112 patent. Prelim. Resp. 12–17.

[5] At this stage of the proceedings, Patent Owner does not present address the merits of Petitioner's contentions. *See generally* Prelim. Resp.

1. Legal Framework

Section 325(d) provides that, in determining whether to institute an *inter partes* review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." The Board uses a two-part framework for evaluating arguments under § 325(d):

> (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and
>
> (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). In applying this framework, we consider the *Becton, Dickinson*[6] factors that address discretion to deny when a petition presents the same or substantially the same prior art or arguments previously presented to the Office, including:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;

[6] *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) ("*Becton, Dickinson*").

> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, Paper 8 at 17–18. Factors (a), (b), and (d), relate to whether the same or substantially the same art or arguments were previously presented to the Office, and factors (c), (e), and (f) relate to whether the petitioner demonstrates that the Office erred in a manner material to the patentability of the claims. *Advanced Bionics*, Paper 6 at 9–11. Only if the same or substantially the same art or arguments were previously presented to the Office do we then consider whether the petitioner has demonstrated a material error by the Office. *Id.*

2. Part One of the Advanced Bionics Framework

Patent Owner asserts that Ueno "was submitted in an IDS during the original prosecution" and "the examiner signed the IDS and initialed the reference indicating that it was considered." Prelim. Resp. 13 (citing Ex. 2001, 132). Patent Owner also asserts that Ueno "appears on the face of the '112 Patent as 'References Cited.'" *Id*. at 13–14 (citing Ex. 1001, 1). We agree with Patent Owner that Ueno was previously presented to the Office during prosecution of the '112 patent. Ex. 1001, code (56); Ex. 2001, 69, 132; *see also* Pet. 25 (Petitioner acknowledging that "Ueno was of record in the '112 patent's prosecution history"). Accordingly, we determine that part one of the *Advanced Bionics* framework is satisfied.

3. Part Two of the Advanced Bionics Framework

Patent Owner contends that the Petition fails to establish that the Office erred in a manner material to the patentability of the challenged claims. Prelim. Resp. 16–17. Petitioner argues that "the Examiner did not describe or address Ueno or apply Ueno substantively in rejecting the claims." Pet. 25.

For the reasons described below, we find that Petitioner has demonstrated a reasonable likelihood of prevailing in showing that at least one claim of the '112 patent is unpatentable over Ueno based on the current record. *See* Section II.E, *infra*; *see also* Section II.A, *supra* (determining that the information presented in the Petition presents a compelling unpatentability challenge). In doing so, Petitioner demonstrates that the Examiner erred in a manner material to the patentability of the challenged claims by not appreciating that Ueno discloses features recited in the claims of the '112 patent lacking in the prior art applied to reject the claims. *See, e.g.*, Ex. 2001, 115–116 (Examiner rejecting a then-pending claim because the applied prior art discloses a second oxide layer that is thicker than the first oxide layer), 140–141 (Applicant arguing in an Amendment After First Action that the applied prior art does not disclose a second oxide layer that is thicker than the first oxide layer as claimed), 157 (Notice of Allowability issued in response to the Amendment After First Action without further comment from the Examiner). Because Petitioner persuasively shows that Ueno discloses the subject matter that the Examiner found missing in the art applied during prosecution, we determine that the Petition establishes that the Office erred in a manner material to the patentability of the challenged claims.

4. Conclusion

Based on our analysis within the *Advanced Bionics* framework, we find that the Petition does not implicate § 325(d) in a manner sufficient to warrant discretionary denial, and we decline to exercise our discretion to deny institution under § 325(d).

C. Level of Ordinary Skill in the Art

Petitioner contends that a person having ordinary skill in the art "would have had the equivalent of a Bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices," and "[l]ess work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa." Pet. 3 (citing Ex. 1002 ¶ 23).

Patent Owner counters that "Petitioner's asserted level of skill in the art is absurdly low given the silicon carbide technology involved in the '112 patent." Prelim. Resp. 7. Instead, Patent Owner asserts that a person having ordinary skill in the art would have had "a Master's degree in electrical engineering or a related subject with a concentration in design and fabrication of silicon carbide power semiconductor devices" or "a Bachelor's degree in electrical engineering or a related subject, in addition to two years of experience in design and fabrication of silicon carbide power semiconductor devices." *Id*. at 7–8. Patent Owner directs us to evidence that "[t]his level of ordinary skill is consistent with the specialized nature of the field of silicon carbide power semiconductor devices." *Id*. at 8 (citing Ex. 2004, x). Patent Owner further advances evidence that the '112 patent inventors, as well as a "few others who were active in the highly specialized field of silicon carbide power devices," possessed backgrounds consistent with Patent Owner's proposed narrower definition of the level of ordinary

skill in the art. Prelim. Resp. 9 (citing Ex. 2007, 1–2; Ex. 2015, 1; Ex. 2016, 1; Ex. 2017, 1–2).

Neither party indicates how the result would change based on our selection of one proposed level of ordinary skill in the art over the other. On this record, we determine that the level of ordinary skill is reflected in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (specific findings on the ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown" (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp*., 755 F.2d 158, 163 (Fed. Cir. 1985))). A more specific definition is not necessary for purposes of deciding whether to institute review, at least because neither party explains how the result would change based on our selection of a definition.

Because, at this stage of the proceeding, our determination as to the level of ordinary skill in the art is preliminary in nature, the parties may wish to address the level of ordinary skill in the art further during trial.

D. Claim Construction

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b) (2019). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

We agree with the parties that no claim term requires express construction for purposes of this Decision. Pet. 34; Prelim. Resp. 10.

E. Asserted Obviousness over Ueno

Petitioner contends that claims 1, 6, 7, 10, and 12 would have been obvious over Ueno. Pet. 35–68.

1. Overview of Ueno

Ueno relates to silicon carbide MOSFETs that serve as power semiconductor devices. Ex. 1003, 1:7–14. Figure 1, reproduced below, is a cross-sectional view of a unit cell of a SiC vertical MOSFET described in Ueno. *Id*. at 7:65–67.

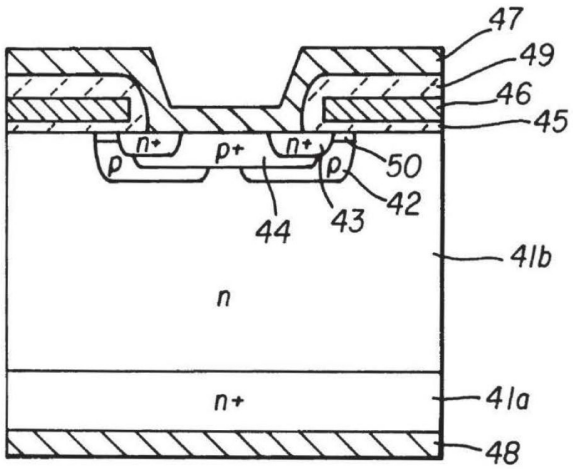


FIG. 1

In the SiC vertical MOSFET depicted in Figure 1, n drift layer 41b is laminated on n^+ drift layer 41a, p base region 42 is formed in a surface layer of n drift layer 41b, and n^+ source region 43 is formed within p base region 42. *Id*. at 8:1–4. High concentration p^+ well region 44 overlaps p base region 42. *Id*. at 8:4–6. Polysilicon gate electrode layer 46 is formed on gate oxide film 45, "over the surface of the p base region 42 that is interposed between the n^+ source region 43 and the exposed surface portion of the n drift layer 41b." *Id*. at 8:6–10. Source electrode 47 is formed in

contact with both n^+ source region 43 and p^+ well region 44, "and a drain electrode 48 is formed on the rear surface of the n^+ drain layer or substrate 41a." *Id*. at 8:10–13. Silicon oxide film 49 is an interlayer insulating film "that insulates the gate electrode layer 46 and the source electrode 47 from each other." *Id*. at 8:13–16.

Ueno explains that its SiC vertical MOSFET "is different from the known SiC vertical MOSFET" in that p base region 42 and n^+ source region 43 "are completely self-aligned, and the interlayer insulating film 49 on the gate electrode layer 46 consists of a Si oxide film." Ex. 1003, 8:34–39.

2. Claim 1

Petitioner asserts, with supporting testimony from Dr. Subramanian, that independent claim 1 is unpatentable as obvious over Ueno. Pet. 35–50; Ex. 1002 ¶¶ 61–84.

a) "A silicon carbide power MOSFET, comprising"

Petitioner contends that Ueno discloses a SiC vertical MOSFET, and also relates to "a method for manufacturing silicon carbide MOS semiconductor devices, such as" MOSFETs, "having a MOS type gate of metal-oxide-semiconductor structure, which use silicon carbide as a semiconductor material and serve as power semiconductor devices." Pet. 36 (quoting Ex. 1003, 1:7–14). Patent Owner does not present arguments in the Preliminary Response addressing the merits of Petitioner's contentions. *See generally* Prelim. Resp. We are persuaded, based on the current record, that Petitioner sufficiently establishes that Ueno teaches "a silicon carbide power MOSFET" as recited in claim 1.

b) "a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof"

Petitioner argues that Ueno "discloses a silicon carbide wafer having an n drift layer 41b grown on substrate 41a," and that "Ueno's drift layer 41b has two (*i.e.*, 'a plurality of') source regions 43 formed adjacent its upper surface." Pet. 36 (citing Ex. 1002 ¶ 64). At this stage of the proceeding, Patent Owner does not address the merits of Petitioner's contentions. *See generally* Prelim. Resp.

(1) "a silicon carbide wafer having a substrate and a drift layer on said substrate"

Petitioner contends that "Ueno specifically discloses a wafer in which a drift layer 41b is grown on an n+ drain layer 41a," and that "Ueno uses 'drain layer' and 'substrate' interchangeably to refer to layer 41a." Pet. 36 (citing Ex. 1003, 8:1–2, 8:12–13, 8:54–55). Petitioner contends that "Ueno also discloses that 'the n drift layer 41b doped with phosphorous is epitaxially grown on the n+ drain layer 41a, to provide a 4H-SiC substrate,'" which a person of ordinary skill in the art would have understood "to mean that both Ueno's drift layer 41b and substrate 41a are made of silicon carbide." *Id*. at 36–37 (citing Ex. 1003, 7:61–67, 8:54–56) (emphasis omitted).

Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "a silicon carbide wafer having a substrate and a drift layer on said substrate."

(2) "said drift layer having a plurality of source regions formed adjacent an upper surface thereof"

Petitioner contends that "Ueno's Figure 1 shows the drift layer 41b having two (*i.e.*, 'a plurality of') source regions 43" that are "formed adjacent an upper surface . . . of the drift layer 41b." Pet. 38 (citing Ex. 1003, 8:11). Petitioner further contends that "Ueno also discloses the formation of the sources adjacent the upper surface" when it teaches "that 'nitrogen (N) ions 5a for forming the n+ source region 43 are implanted' and notes that" in Ueno's Figure 2g, "'reference numeral 5b denotes nitrogen atmos [*sic*] thus implanted.'" *Id*. at 39 (citing Ex. 1003, 9:59–62, Fig. 2g). According to Petitioner, Ueno's Figure 2g illustrates that "the nitrogen atoms 5b are adjacent the upper surface of the drift layer 41b." *Id*. (citing Ex. 1002 ¶ 68).

Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches the "said drift layer having a plurality of source regions formed adjacent an upper surface thereof" limitation of claim 1.

c) "a plurality of polysilicon gates above said drift layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions, said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region"

Petitioner contends that "Ueno explicitly discloses two (*i.e.*, 'a plurality of') gates above the drift layer 41b," each of which "is adjacent a corresponding one of the two source regions 43." Pet. 40 (citing Ex. 1003, 8:6–9, Fig. 1). Petitioner further contends that "Ueno's Figure 1 illustrates that the right gate (*i.e.*, 'said first gate') has a top surface, a lower surface,

and a sidewall that overlies the right source region 43 (*i.e.*, 'said first source region')." *Id*. (citing Ex. 1002 ¶ 71) (emphases omitted). At this stage of the proceeding, Patent Owner does not address the merits of Petitioner's contentions. *See generally* Prelim. Resp.

(1) "a plurality of polysilicon gates above said drift layer"

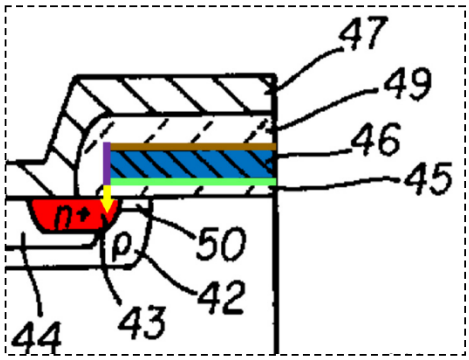
Petitioner contends that Ueno's Figure 1 shows two gates above drift layer 41b, and teaches "that 'polysilicon film 1c is patterned by photolithography, to provide the gate electrode layer 46.'" Pet. 41 (citing Ex. 1003, 8:6, 8:8–9, 10:42–44, Figs. 1, 3c, 3d). Petitioner further contends that "[t]he patterning of polysilicon film 1c into individual structures 46, as Ueno shows in Figure 3d, forms polysilicon gates." *Id*. Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "a plurality of polysilicon gates above said drift layer."

(2) "said plurality of polysilicon gates including a first gate adjacent a first of said source regions"

Petitioner contends that "[e]ach of the two gates that Ueno illustrates in Figure 1 is adjacent a corresponding one of the two source regions 43." Pet. 42; Ex. 1002 ¶ 74. Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "said plurality of polysilicon gates including a first gate adjacent a first of said source regions."

(3) "said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region"

Petitioner provides an annotated version of a section of Ueno's Figure 1, reproduced below, to illustrate its contentions with respect to this limitation.



EX1003, FIG. 1
(excerpted and annotated)

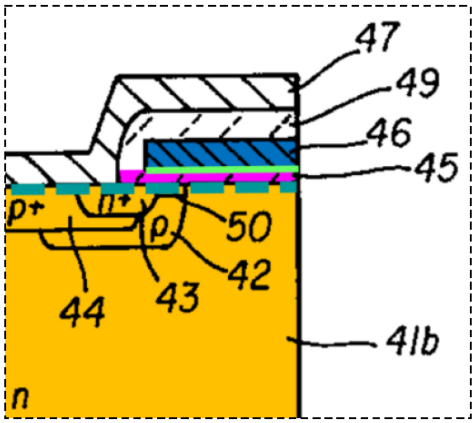
Annotated Figure 1 depicts the top right corner of a cross-sectional view of a part of a SiC vertical MOSFET according to an embodiment described in Ueno, in which gate 46 is shaded blue, a brown line is added on the top of gate 46, a purple line is added on the left side of gate 46, and a lime-colored line is added on the bottom of gate 46, source region 43 is shaded red, and a yellow arrow extends from the bottom of the purple line into source region 43. Pet. 44; Ex. 1003, 7:31–33. Petitioner contends that "the right gate (*i.e.*, 'said first gate') has a top surface (outlined in brown), a lower surface (outlined in lime), and a sidewall (outlined in purple)." *Id*. at 42–43 (emphasis omitted). Petitioner also contends that, "[a]s further illustrated by the yellow arrow, the sidewall overlies the right source region 43 (*i.e.*, 'said first source region')." *Id*. at 43. Petitioner further contends that, although "Ueno does not provide a textual description" of the side wall overlying the source region, a person of ordinary skill in the art would have found it obvious to do because "[i]t was well known in the art to provide alignment

tolerance by adding gate-source overlap, to account for the imperfect alignment that is possible in real manufacturing processes." *Id*. at 43–44. Petitioner contends that "because of the standard practice of providing an overlap for alignment tolerance, even without textual description of the gate overlying the source by Ueno, it would have been obvious for the gate to have a sidewall overlying the source." *Id*. at 44.

Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region."

d) "a first oxide layer between said first gate lower surface and said upper surface of said drift layer"

Petitioner provides an annotated version of a section of Ueno's Figure 1, reproduced below, to illustrate its contentions with respect to this limitation.



EX1003, FIG. 1
(excerpted and annotated)

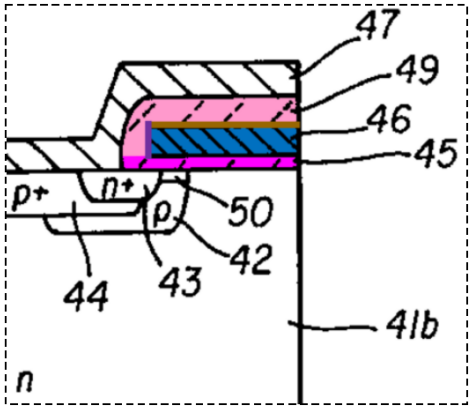
Annotated Figure 1 depicts the top right corner of a cross-sectional view of a part of a SiC vertical MOSFET according to an embodiment described in Ueno, in which gate 46 is shaded blue, gate oxide film 45 is shaded magenta, a lime-colored line is added between the bottom of gate 46 and gate oxide

film 45, drift layer 41b is shaded orange, and a dashed teal line is added along the top of drift layer 41b. Pet. 44–45 (citing Ex. 1003, 8:7). Petitioner contends that gate oxide film 45 is "a first oxide layer" that is located between the lower surface (indicated by the lime-colored line) of gate 46 ("said first gate") and the upper surface (indicated by the dashed teal line) of drift layer 41b. *Id*. Petitioner contends that Ueno describes the steps for manufacturing the MOSFET depicted in Figure 1, explaining "'an oxide film 6d that . . . provides the gate oxide film 45 is formed,' followed by the deposition of the polysilicon film 1c that provides the gates," and that "oxide film 6d is formed on the upper surface of the drift layer 41b and is covered by the polysilicon film 1c, which is subsequently patterned to form the gates." *Id*. at 45 (citing Ex. 1003, 7:37–39, 10:35–40, Figs. 3c, 3d). Therefore, according to Petitioner, "the gate oxide film 45 is between the lower surface of the right gate and the upper surface of the drift layer 41b." *Id*. at 45–46 (citing Ex. 1002 ¶ 77).

Patent Owner does not present arguments in the Preliminary Response addressing the merits of Petitioner's contentions. *See generally* Prelim. Resp. Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "a first oxide layer between said first gate lower surface and said upper surface of said drift layer."

e) "a second thicker oxide layer over said top surface and sidewall of said first gate; and"

Petitioner provides an annotated version of a section of Ueno's Figure 1, reproduced below, to illustrate its contentions with respect to this limitation.



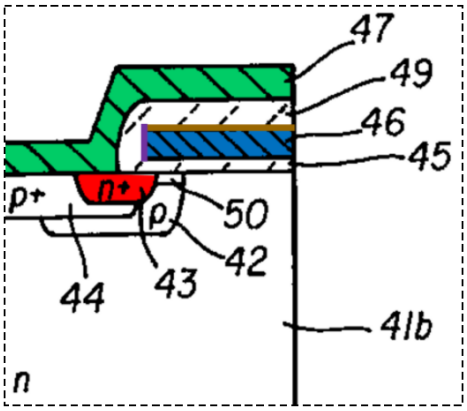
EX1003, FIG. 1

Annotated Figure 1 depicts the top right corner of a cross-sectional view of a part of a SiC vertical MOSFET according to an embodiment described in Ueno, in which gate 46 is shaded blue, gate oxide film 45 is shaded magenta, a brown line is added on the top of gate 46, a purple line is added on the left side of gate 46, and interlaying insulating film 49 is shaded pink. Pet. 46. Petitioner contends that annotated Figure 1 "illustrates the interlayer insulating film 49 ('a second oxide layer') over the top surface (outlined in brown) and the sidewall (outlined in purple) of the right gate (*i.e.*, 'said first gate')." *Id*. (emphases omitted). Petitioner also contends that interlayer insulating film 49 is thicker than gate oxide film 45, because Ueno teaches that gate oxide film 45 is 0.5 μm thick, and interlayer insulating film 49 is 2 μm. *Id*. at 48–49 (citing Ex. 1003, 8:29–32; Ex. 1002 ¶ 81).

Patent Owner does not present arguments in the Preliminary Response addressing the merits of Petitioner's contentions. *See generally* Prelim. Resp. Having reviewed Petitioner's contentions and the evidence of record at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "a second thicker oxide layer over said top surface and sidewall of said first gate."

f) "a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region"

Petitioner provides an annotated version of a section of Ueno's Figure 1, reproduced below, to illustrate its contentions with respect to this limitation.



EX1003, FIG. 1
(excerpted and annotated)

Annotated Figure 1 depicts the top right corner of a cross-sectional view of a part of a SiC vertical MOSFET according to an embodiment described in Ueno, in which gate 46 is shaded blue, a brown line is added on the top of gate 46, a purple line is added on the left side of gate 46, source region 43 is shaded red, and source electrode layer 47 is shaded green. Pet. 49–50 (citing Ex. 1003, 8:10–11, 10:62–63). Petitioner contends that annotated Figure 1 shows that "source electrode 47 conformally and laterally extends across the top surface (outlined in brown) and sidewall (outlined in purple) of the right gate (*i.e.*, 'said first gate') and the right source region 43 (*i.e.*, 'said adjacent first source region.')". *Id*. at 49 (emphases omitted).

Patent Owner does not present arguments in the Preliminary Response addressing the merits of Petitioner's contentions. *See generally* Prelim. Resp. Having reviewed Petitioner's contentions and the evidence of record

at this stage of the proceeding, we are persuaded that Petitioner sufficiently establishes that Ueno teaches "a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region."

g) Conclusion

Having reviewed Petitioner's contentions regarding independent claim 1, as well as the cited portions of Ueno and the Subramanian Declaration, we determine that Petitioner has demonstrated a reasonable likelihood of establishing that independent claim 1 would have been obvious over Ueno.

3. Claims 6, 7, 10, and 12

Petitioner asserts, with supporting testimony from Dr. Subramanian, that independent claim 6 is unpatentable as obvious over Ueno. Pet. 51–63; Ex. 1002 ¶¶ 61–84. Petitioner alleges that Ueno teaches or suggests every limitation of claim 6 as follows:

Preamble: "A MOSFET structure, comprising:" (Pet. 51 (relying on Ex. 1002 ¶ 86; Pet. 35–36));

Element 6[a]: "a silicon carbide wafer having a substrate body with an upper surface, said substrate body having at least one source region formed adjacent said upper surface" (Pet. 51–54 (relying on Ex. 1003, 8:1–4, 8:11–13, 8:54–55, 9:59–62, 10:21–24, Figs. 1, 2g; Ex. 1002 ¶¶ 87–93; Pet. 36–38));

Element 6[b]: "a substrate surface oxidation layer on said upper surface of said substrate body and adjacent said source region" (Pet. 55–56 (relying on Ex. 1003, 7:37–39, 8:7, 10:35–36, Figs. 1, 3c, 3d; Ex. 1002 ¶¶ 94–95));

Element 6[c]: "at least two polysilicon gates above said substrate surface oxidation layer, said gates each having a top, a bottom, and sides, wherein a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates" (Pet. 56–60 (relying on Ex. 1003, 7:37–39, 7:65–67, 8:6–10, 8:32–33, 10:21–24, 10:42–44, 10:48–61, Figs. 1, 3e, 3f; Ex. 1002 ¶¶ 96–101; Ex. 1009, 70–73, 455, Figs. 3.9, 3.9a; Pet. 46–49));

Element 6[d]: "a gate oxide layer, thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates; and" (Pet. 61–62 (relying on Ex. 1003, 7:37–39, 10:48–61, Figs. 3e, 3f; Ex. 1002 ¶¶ 102–103; Pet. 49–50));

Element 6[e]: "a material layer over said first source region and between said gate oxide layers on said sides of said gates, said material layer comprising one of an oxide and a metal contact." (Pet. 62–63 (relying on Ex. 1002 ¶¶ 104–105; Ex. 1003, Fig. 1; Pet. 49–50)).

Patent Owner does not present arguments in the Preliminary Response addressing the merits of Petitioner's contentions. *See generally* Prelim. Resp.

Having reviewed Petitioner's contentions regarding independent claim 6, as well as the cited portions of Ueno and the Subramanian Declaration, we determine that Petitioner has demonstrated a reasonable likelihood of establishing that independent claim 6 would have been obvious over Ueno. We have also considered the arguments and evidence with respect to claims 7, 10, and 12 that depend, directly or indirectly, from claim 6. Pet. 63–68; Ex. 1002 ¶¶ 106–113. At this stage of the proceeding, based on the record before us, we are persuaded that Petitioner establishes a reasonable likelihood of prevailing as to claims 7, 10, and 12 as well.

F. Asserted Obviousness over Ueno and Lidow

Petitioner contends that claim 11 would have been obvious over the combined teachings of Ueno and Lidow. Pet. 68–82; Ex. 1002 ¶¶ 114–133. At this stage of the proceeding, Patent Owner does not address the merits of Petitioner's contentions. *See generally* Prelim. Resp. Having determined that Petitioner establishes a reasonable likelihood of showing that at least one of the challenged claims is unpatentable, we institute an *inter partes* review with respect to this ground as well. *See Guidance of the Impact of SAS on AIA Trial Proceedings* (April 26, 2018) (explaining that "the PTAB will institute as to all claims or none" and "if the PTAB institutes a trial, the PTAB will institute on all challenges raised in the petition").

III. CONCLUSION

Based on the arguments in the Petition and the Preliminary Response, and the evidence of record, we determine that Petitioner demonstrates a reasonable likelihood that it will prevail on its challenge to at least one of the challenged claims of the '112 patent. Thus, we institute an *inter partes* review of all challenged claims on all the grounds presented.

The factual findings set forth in this Decision are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. See *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that "there is a significant difference between a petitioner's burden to establish a 'reasonable likelihood of success' at institution, and actually proving invalidity by a preponderance of the evidence at trial") (quoting 35 U.S.C. § 314(a) and comparing *id*. with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review of claims 1, 6, 7, and 10–12 of the ’112 patent is instituted with respect to the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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