United States Court of Appeals for the Federal Circuit

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Plaintiff-Appellee

v.

BROADCOM LIMITED, NKA BROADCOM INC., BROADCOM CORPORATION, AVAGO TECHNOLOGIES LIMITED, NKA AVAGO TECHNOLOGIES INTERNATIONAL SALES PTE. LIMITED, APPLE INC.,
Defendants-Appellants

2020-2222, 2021-1527

Appeals from the United States District Court for the Central District of California in No. 2:16-cv-03714-GW-AGR, Judge George H. Wu.

Decided: February 4, 2022

KATHLEEN M. SULLIVAN, Quinn Emanuel Urquhart & Sullivan, LLP, Los Angeles, CA, argued for plaintiff-appellee. Also represented by JAMES R. ASPERGER; BRIAN P. BIDDINGER, EDWARD J. DEFRANCO, New York, NY; TODD MICHAEL BRIGGS, KEVIN P.B. JOHNSON, Redwood Shores, CA; DEREK L. SHAFFER, Washington, DC; KEVIN ALEXANDER SMITH, San Francisco, CA.

WILLIAM F. LEE, Wilmer Cutler Pickering Hale and Dorr LLP, Boston, MA, argued for defendants-appellants. Also represented by LAUREN B. FLETCHER, MADELEINE C. LAUPHEIMER, JOSEPH J. MUELLER; STEVEN JARED HORN, DAVID P. YIN, Washington, DC; MARK D. SELWYN, Palo Alto, CA.

Before LOURIE, LINN, and DYK, *Circuit Judges*.

Opinion for the Court filed by *Circuit Judge* LINN.

Opinion concurring-in-part and dissenting-in-part filed by *Circuit Judge* DYK.

LINN, *Circuit Judge*.

Broadcom Limited, Broadcom Corporation, and Avago Technologies Ltd. (collectively "Broadcom") and Apple Inc. ("Apple") appeal from the adverse decision of the District Court for the Central District of California in an infringement suit filed by the California Institute of Technology ("Caltech") for infringement of its U.S. Patents No. 7,116,710 ("the '710 patent"), No. 7,421,032 ("the '032 patent"), and No. 7,916,781 ("the '781 patent").

Because the district court did not err in its construction of the claim limitation "repeat" and because substantial evidence supports the jury's verdict of infringement of the asserted claims of the '710 and '032 patents, we affirm the district court's denial of JMOL on infringement thereof. We also affirm the district court's conclusion that claim 13 of the '781 patent is patent-eligible but vacate the jury's verdict of infringement thereof because of the district court's failure to instruct the jury on the construction of the claim term "variable number of subsets." We thus remand for a new trial on infringement of claim 13 of the '781 patent. We further affirm the district court's summary judgment findings of no invalidity based on IPR estoppel and its determination of no inequitable conduct. We affirm the

district court's decision with respect to its jury instructions on extraterritoriality. But because Caltech's two-tier damages theory cannot be supported on this record, we vacate the jury's damages award and remand for a new trial on damages.

BACKGROUND

I. The Caltech Patents

Caltech's '710 and '032 patents disclose circuits that generate and receive irregular repeat and accumulate ("IRA") codes, a type of error correction code designed to improve the speed and reliability of data transmissions. Wireless data transmissions are ordinarily susceptible to corruption arising from noise or other forms of interference. IRA codes help to identify and correct corruption after it occurs.

The encoding process begins with the processing of data before it is transmitted. The data consists of information bits in the form of 1's and 0's. The information bits are input into an encoder, a device that generates codewords comprised of parity bits and the original information bits. Parity bits are appended at the end of a codeword. Codewords are created in part by repeating information bits in order to increase the transmission's reliability. When noise or other forms of interference introduce errors into the codewords during transmission, the decoder identifies these errors and relies on the codeword's redundant incorporation of the original string of information bits to correct and eliminate the errors.

Before Caltech's patents, error correction codes had already incorporated repetition and irregular repetition. These codes, however, were less than optimally efficient because they were either encoded or decoded in quadratic time, which meant that the number of computations

required to correct a given number of bits far exceeded the number of bits ultimately corrected.

In the '710 and '032 patents, the IRA codes are linear-time encodable and decodable, rather than quadratic. '710 patent, col. 2, ll. 6–7 ("The encoded data output from the inner coder may be transmitted on a channel and decoded in linear time."); *id.* col. 2, l. 59 ("The inner coder 206 may be a linear rate-1 coder."); *id.* col. 3, ll. 25–26 ("An IRA code is a linear code."). Using a linear code means that the relationship between the bits corrected and the computations required is directly proportional. Minimizing the number of calculations that an encoder or decoder must perform permits smaller, more efficient chips with lower power requirements.

The claimed improvement involves encoding the information bits through a process of irregular repetition, scrambling, summing, and accumulation. Repeating inputted information bits is necessary to increase the reliability of data transmissions, and irregular repetition minimizes the number of times that information bits are repeated. Minimizing the number of times that an information bit is repeated is crucial to the efficiency of the claimed inventions because the repetitions impact the device's coding rate or speed, as well as the code's complexity. The fewer repeated bits there are, the fewer number of computations that an encoder must perform, which in turn permits smaller circuits, decreased power requirements, and decreased operating temperatures in devices incorporating the circuits.

The claims and accompanying specifications of the Caltech patents make clear that each inputted information bit must be repeated. The parties agree that every claim at issue requires irregular repetition of information bits either explicitly or via the court's construction. This is so even where the irregular repetition is not expressly

required by the claims. For example, the agreed-upon construction of a Tanner graph in the '032 patent requires that "every message bit is repeated . . . ." J. App'x 33. Furthermore, the claims and accompanying specifications make clear that each bit must be repeated irregularly, stating, for example in the '710 patent, "a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times." '710 patent, col. 2, ll. 53–58.

The '781 patent discloses and claims a method for creating codewords in which "information bits appear in a variable number of subsets." Before trial, Apple and Broadcom sought summary judgment that claim 13 was unpatentable under 35 U.S.C. § 101. After finding that the claims were directed to a patent-eligible subject matter (step 1 of *Alice*[1])—a method of performing error correction and detection encoding with the requirement of irregular repetition—the court declined to reach whether they contained an inventive concept (step 2 of *Alice*). To support patentability, Caltech argued that the "variable number of subsets" language required irregular information bit repetition. The district court agreed and adopted and relied on Caltech's interpretation to deny summary judgment of unpatentability. No party on appeal challenges this claim interpretation.

II. The Accused Products

Caltech alleged infringement by certain Broadcom Wi-Fi chips and Apple products incorporating those chips, including smartphones, tablets, and computers. The accused Broadcom chips were developed and supplied to Apple pursuant to Master Development and Supply Agreements

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[1] Alice Corp. Pty. Ltd. v. CLS Bank Int'l, 573 U.S. 208 (2014).

negotiated and entered into in the United States. Caltech specifically identified as infringing products two encoders contained in the Broadcom chips—a Richardson-Urbanke ("RU") encoder and a low-area ("LA") encoder. In the accused encoders, incoming information bits are provided to AND gates in the RU encoder or multiplexers in the LA encoder.

Throughout the trial and on appeal, the parties treated AND gates and multiplexers as functionally identical for all relevant issues. It thus suffices to describe in detail the RU encoder only. In the RU encoder, each information bit is simultaneously fed as one input to 972 separate AND gates. Each AND gate receives a second input—a "parity-check" or "enable" bit of 0 or 1—derived from a low-density parity check matrix. This matrix is an array of 1's and 0's. A low-density parity check matrix is one in which the number of 1's in the matrix is significantly fewer than the number of 0's.

In its brief, Broadcom presents the following table, using the example of the functioning of a single AND gate, to show how outputs are determined by the two inputs:

Input 1 (Information Bit)	**Input 2 (Parity-Check Bit)**	**AND Gate Output**
0	0	0
0	1	0
1	0	0
1	1	1

For each AND gate, the output of the gate is 1 if both inputs (the information bit *and* the parity-check bit) are 1; otherwise, the output is 0. One consequence of this logic is that if the parity-check bit is 1 (as shown in rows two and four), then the output *is identical to* the information-bit input. If the parity-check bit is 0, the output is 0, regardless

of the value of the input (rows one and three). Throughout trial, the parties referred to parity-check bits and enable bits interchangeably. Parity-check bits determine the action of the AND gates, which are open/on when the parity-check bit is 1 and closed/off when the parity-check bit is 0.

Caltech sued Broadcom and Apple on May 26, 2016, alleging infringement under 35 U.S.C. § 271 by Broadcom wireless chips and Apple products incorporating those chips. Both defendants denied that any of the accused devices infringed Caltech's patents, and in turn asserted counterclaims for declaratory judgment of non-infringement, invalidity under 35 U.S.C. §§ 101, 102, 103, and/or 112, and unenforceability due to inequitable conduct.

III. Pre-Trial Proceedings

Before trial, Apple filed multiple IPR petitions challenging the validity of the claims at issue, relying on various prior art references. The Patent Trial and Appeal Board ("PTAB" or "Board") issued a number of written decisions, which concluded that Apple failed to show the challenged claims were unpatentable as obvious. Before the district court, Apple and Broadcom argued that the asserted claims would have been obvious over new combinations of prior art not asserted in the IPR proceedings.

The district court granted summary judgment of no invalidity, interpreting 35 U.S.C. § 315(e)(2) as precluding parties from raising invalidity arguments at trial that they reasonably could have raised in their IPR petitions. It also denied the motion filed by Apple and Broadcom for summary judgment of invalidity under 35 U.S.C. § 101 for the '781 patent. The district court granted Caltech's summary judgment motion as to inequitable conduct, finding no inequitable conduct with respect to Caltech's failure to disclose Richardson99 during prosecution. The district court reasoned that this prior art reference was not but-for material to the PTO's grant of Caltech's patents.

The district court also conducted a *Markman* hearing and initially construed the claim limitation "repeat." That construction is germane to all of the asserted claims. At the conclusion of the *Markman* hearing, the district court construed "repeat" to have its plain and ordinary meaning. The district court noted that the repeated bits "are a construct distinct from the original bits from which they are created," but that they need not be generated by storing new copied bits in memory.

IV Trial Proceedings

A. Infringement of the '710 and '032 Patents

At trial, Caltech argued that the accused chips infringed claims 20 and 22 of the '710 patent and claims 11 and 18 of the '032 patent. Both groups of claims explicitly require irregular repetition; i.e., repetition of groups of information bits an irregular number of times. Claims 20 and 22 of the '710 patent depend from claim 15, which claims:

> 15. A coder comprising: a first coder having an input configured to receive a stream of bits, said first coder operative to repeat said stream of bits irregularly and scramble the repeated bits; and a second coder operative to further encode bits output from the first coder at a rate within 10% of one.

'710 patent, col. 8, ll. 1–6. Claims 11 and 18 of the '032 patent cover devices for encoding and decoding pursuant to a Tanner graph:[2]

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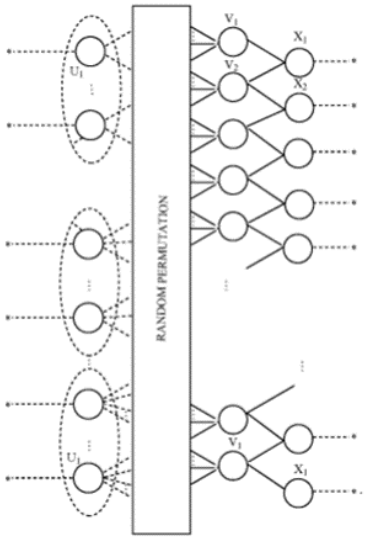
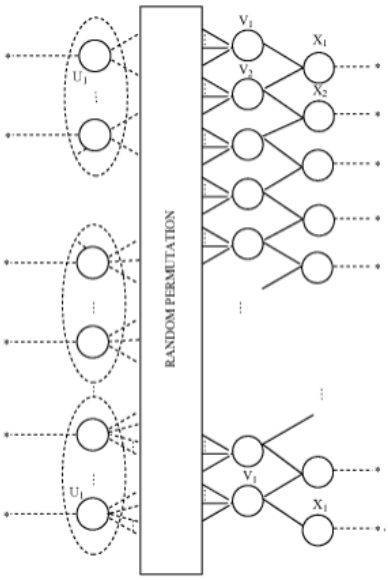
[2] During claim construction, the parties agreed that a Tanner graph is a visual representation of the "constraints that determine the parity bits" created by an IRA code. J. App'x 33.

11. A device comprising: an encoder configured to receive a collection of message bits and encode the message bits to generate a collection of parity bits in accordance with the following Tanner graph:



18. A device comprising: a message passing decoder configured to decode a received data stream that includes a collection of parity bits, the message passing decoder comprising two or more check/variable nodes operating in parallel to receive messages from neighboring check/variable nodes and send updated messages to the neighboring variable/check nodes, wherein the message passing decoder is configured to decode the received data stream that has been encoded in accordance with the following Tanner graph:



'032 patent, col. 8, l. 63–col. 9, l. 34; col. 9, l. 57–col. 10, l. 42. The district court's claim construction ruling required that the Tanner graphs in claims 11 and 18 also perform repetition. J. App'x 33 (defining Tanner graph as a depiction of "an IRA code as a set of parity checks where every message bit is repeated, at least two different subsets of message bits are repeated a different number of times"). No party challenges this construction on appeal.

During trial, the district court revisited and clarified its earlier claim construction ruling of the term "repeat" and instructed the jury that repeat means "generation of additional bits, where generation can include, for example, duplication or reuse of bits." Apple and Broadcom then argued that the chips did not infringe the '710 and '032 patents because they did not repeat information bits at all, much less irregularly. The jury ultimately found infringement of all the asserted claims. Broadcom and Apple filed post-trial motions for JMOL and a new trial, challenging the jury's infringement verdict. The district court denied JMOL, finding no error in its claim construction ruling and

concluding that the verdict was supported by substantial evidence.

B. Infringement of the '781 Patent

At trial, Caltech also argued that the accused chips infringed claim 13 of the '781 patent. That patent discloses and claims a method for creating codewords in which "information bits appear in a variable number of subsets." Claim 13 recites:

> A method of encoding a signal, comprising:
>
> receiving a block of data in the signal to be encoded, the block of data including information bits; and
>
> performing an encoding operation using the information bits as an input, the encoding operation including an accumulation of mod-2 or exclusive-OR sums of bits in subsets of the information bits, the encoding operation generating at least a portion of a codeword,
>
> wherein the information bits appear in a variable number of subsets.

'781 patent, col. 8, ll. 7–16.

Despite its construction at the summary judgment stage that the claim term "variable number of subsets" requires irregular information bit repetition, the district court declined to provide the jury with an instruction of that claim construction determination and the jury determined that Apple and Broadcom infringed claim 13 of the '781 patent. Broadcom and Apple filed JMOL and new trial motions arguing that the district court erred in refusing their requested instruction and that JMOL of noninfringement was appropriate because the irregular repetition requirement was not satisfied. In denying these post-trial motions, the district court concluded that it was "within its

discretion" not to issue this instruction so as not to "confuse the record on this issue."

C. Damages

To compensate for Broadcom and Apple's infringement, Caltech proposed a two-tier damages theory, which sought different royalty rates from each of the infringers despite the fact that liability arose from the same accused technology in the same chips. Even though the district court voiced its discomfort with the two-tier theory, it allowed Caltech to present the theory to the jury, which relied on it to award Caltech $270,241,171 for Broadcom's infringement and $837,801,178 for Apple's infringement. The jury's damages award was based on Caltech's experts' testimony, admitted over Broadcom and Apple's objection. Appellants challenged the damages award in their post-trial motions, which the district court denied. The district court entered judgment against Broadcom totaling $288,246,156, and against Apple totaling $885,441,828. These awards included pre-judgment interest, as well as post-judgment interest and an ongoing royalty at the rate set by the jury's verdict.

Broadcom and Apple appeal. We have jurisdiction pursuant to 28 U.S.C. §1295(a)(1).

DISCUSSION

I. Standard of Review

Claim construction is reviewed de novo when relying on intrinsic evidence. *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 333 (2015). Infringement and damages are reviewed for substantial evidence. *Lucent Techs., Inc. v. Gateway, Inc.*, 580 F.3d 1301, 1309, 1324 (Fed. Cir. 2009). Statutory interpretation is reviewed de novo. *Power Integrations v. Semiconductor Components Indus., LLC*, 926 F.3d 1306, 1313 (Fed. Cir. 2019). Patent-eligibility under 35 U.S.C. § 101 is reviewed de novo. *Recognicorp, LLC*

v. Nintendo Co., 855 F.3d 1322, 1326 (Fed. Cir. 2017). We review patent jury instructions on patent law issues de novo, asking if the instructions were legally erroneous and prejudicial. *Bettcher Indus., Inc. v. Bunzl USA, Inc.*, 661 F.3d 629, 638-39 (Fed. Cir. 2011).

We review a district court's order denying JMOL under the standard applied by the regional circuit. *Apple, Inc. v. Samsung Electronics Co., Ltd.*, 839 F.3d 1034, 1040 (Fed. Cir. 2016). In the Ninth Circuit, JMOL "is proper when the evidence permits only one reasonable conclusion and the conclusion is contrary to that of the jury." *See Monroe v. City of Phoenix*, 248 F.3d 851, 861 (9th Cir. 2001). The Ninth Circuit explains that "[t]he evidence must be viewed in the light most favorable to the nonmoving party, and all reasonable inferences must be drawn in favor of that party." *Id*. The Ninth Circuit reviews a district court's decision to deny JMOL de novo. *Id*.

II. Infringement

A. The '710 and '032 Patents

Broadcom and Apple argue that the district court erroneously construed "repeat," contending that the accused AND gates and multiplexers do not "repeat" information bits in the manner claimed, but instead *combine* the information bits with bits from a parity-check matrix to output *new* bits reflecting that combination. Broadcom and Apple further argue that the AND gates and multiplexers also do not generate bits "irregularly," asserting that they output the *same* number of bits for every information bit. Caltech argues in response that expert testimony throughout the record establishes that every information bit is repeated an irregular number of times. According to Caltech, the jury heard testimony explaining that in the RU devices *every* bit in the stream of information bits is fed by wire simultaneously to the information inputs of *all* 972 AND gates and that at any time, at least 3 and up to 12 of those AND gates

will be enabled *to repeat that bit* at the output of the AND gates. We find no error in the district court's construction of the term "repeat" and agree with Caltech that substantial evidence in the record supports the jury's verdict on infringement.

1. Claim Construction of "repeat"

The district court construed "repeat" to mean "generation of additional bits, where generation can include, for example, duplication *or reuse of bits*" (emphasis added). J. App'x 171. Broadcom and Apple argue that that construction is inconsistent with the claim language, the specification and the construction given by another judge in a different case.[3] Caltech argues in response that the plain claim language requiring repeating information bits does not require generating new, distinct bits and that the district court was correct in construing the term to not exclude the reuse of bits. We agree with Caltech.

The district court correctly observed that the claims require repeating but do not specify how the repeating is to occur: "The claims simply require bits to be repeated, without limiting how specifically the duplicate bits are created or stored in the memory." J. App'x 10. The specifications confirm that construction and describe two embodiments, neither of which require duplication of bits. The district court carefully and fully considered both the language of the claims and that of the written description and faithfully applied our precedent to reach the construction made during the trial and presented to the jury. We are not

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[3] Broadcom and Apple misplace reliance on the construction of the term "repeat" made on an undeveloped record in the context of a summary judgment motion. *See California Institute of Technology v. Hughes Communications Inc.*, 35 F. Supp. 3d 1176 (C.D. Cal. 2014).

persuaded that the district court erred in construing the term "repeat" and, therefore, affirm the same.

2. JMOL on Infringement

Broadcom and Apple argue that the evidence before the jury on infringement permitted only one verdict, namely no infringement, and that the district court erred in denying JMOL. Broadcom and Apple put forth two rationales for noninfringement of the "irregular repeat" requirement, Appellant's Br. 27–31. First, looking at each gate alone and commenting on the "repeat" requirement, they argue that the AND gate does not "repeat" the inputted information bit "because the AND gate's output depends on not only the information bit but *also* the parity-check-matrix bit." Appellant's Br. 29. Second, focusing on the "irregular" half of "irregular repeat," they argue that "even if the outputted bits could be deemed 'repeats' of the information bits," "any repetition is not 'irregular' because each information bit leads to the *same number* of outputted bits." Appellant's Br. 30.

Caltech argues in response that the jury was provided with substantial evidence to support the verdict of infringement and that the district court correctly denied JMOL. Caltech asserts that the fact that an AND gate doesn't have an information-bit/output match for *every* information bit hardly means that it isn't repeating *any* information bit. Appellee's Br. 21–22 (citing J. App'x 3036–38). All that matters, according to Caltech, is that *sometimes* there is such a match that qualifies as a "repeat," so long as each and every bit is repeated at least once. Caltech argues that Broadcom ignores ample expert testimony, which the jury could credit, that sometimes an AND gate repeats an information bit and that, taking the 972 AND gates together, the carefully designed parity-bit table/matrix meant that "the products output and store information bits between two and twelve times." Appellee's Br. 22. Caltech asserts

that, considering the system *as a whole*, each information bit is in fact repeated, and they are not all repeated the same number of times. We agree with Caltech.

Caltech's expert, Dr. Matthew Shoemake began his testimony with reference to the exemplary table reproduced above. *See* J. App'x 3036–38. He explained that in the parity-check-bit-equals-1 situation (second and fourth rows of the table), the output bit is a "repeat" of the information-bit input. Where the parity-check bit is 1, the gate affirmatively enables the information bit to be duplicated as the output bit. That is a "repeat." That is so, he explained, because the information bit in that situation "flows through" to appear again in the output. He also addressed the one other situation where the output bit is identical to the information bit, namely, in the first row of the above table, where both the information bit and the parity-check bit are 0, and so is the output. Despite the identity of the information bit and the output bit, he explained, that situation does *not* involve a "repeat." A 0 parity-check bit turns *every* information bit (0 or 1) into a 0 output, so the output bit in that situation *tells one nothing about* the information bit. Since the whole point of this encoding scheme is to use outputs that *give information about* the information bits, a 0 parity-check bit does not produce a "repeat" even when the information-bit input and the output are the same. Broadcom's expert, Dr. Wayne Stark, expressly recognized that this was exactly what Dr. Shoemake said in his testimony. J. App'x 3956 ("He said it's a repeat only if the enable [parity-check] signal is a one and it's not a repeat if an enable [parity-check] symbol is a zero.").

Dr. Shoemake also explained to the jury that "flow through" means that the information bit is repeated at the output gate. *See*, *e.g.*, J. App'x 2810, 2812, 3017–19. When the information bit "flows through" to the output gate because the parity-check bit is 1, that's a repeat, both according to the expert's usage and a plain understanding of the

word "repeat." *See, e.g.*, J. App'x 3038. When the information bit is not allowed to flow through (because the parity-check bit is 0), that's not a repeat (even though both the information bit and the output bit are 0).[4]

In explaining the operation of the RU encoder itself, Dr. Shoemake testified that it contains "972 mac_reg modules [AND gates], and the information bits are connected to every single one of them." J. App'x 2831. He further testified that: "[D]epending on which information bit it is, 3 to 12 of these gates are enabled which then allows 3 to 12 … [information bits] to flow through 3 to 12 times and since that number varies, there's irregular repetition," J. App'x 3034-35; "[W]hat really happens in the accused products, the tables tell you how many times should information bit number one be repeated. And the tables I've mentioned several times that they allow information bits, and I should force information bits to be repeated between 3 and 12 times," J. App'x 3080; and "[T]he information bit starts off in one location in the chip, and then it's connected to 972 distinct locations so it can be irregularly repeated in this architecture." J. App'x 3018.

Dr. Shoemake's position was consistent throughout his testimony: the physical connection of the first inputs of all 972 AND gates for simultaneous receipt of the information bit stream *and* the connection of the parity-bit system to the other inputs of the AND gates to selectively enable 3 to 12 of those gates at any time *together* implement irregular

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[4] Caltech's Red Brief incorrectly cited this example as representing a repeat. Red. Br. 21. This was evidently error, given that it directly contracted the directly cited pages of Dr. Shoemake's testimony. This error does not, however, change the fact that Caltech correctly identified the substantial trial testimony on which the jury could base its decision.

repetition. Dr. Shoemake explained that this is exactly what one sees when one looks at the "overall architecture" ("whole architecture"), *not* each gate alone. J. App'x 3031, 3035, 3038. As he specifically testified:

> Q: Your position, your opinion . . . is that that branch wire creates 972 repeat bits within the meaning of the claims in the Caltech patents; correct?
>
> > A: So based on my analysis, this wire going to the Mac rag modules and the AND gates under control of the tables that are stored in the RU encoder actually allows the information bits to flow through [a] different number of times. *It's always 3 to 12 times for a particular information bit*. And so [i]n my analysis, this is exactly how the RU encoder is implementing irregular repetition of information bits.

J. App'x 3019 (emphasis added).

For the foregoing reasons, substantial evidence supports the jury's verdict of infringement of the '710 and '032 patents. We are not persuaded that the record before the jury permits only a verdict of no infringement. We therefore affirm the district court's denial of JMOL.

B. The '781 Patent

1. Patent Eligibility

Broadcom and Apple contend that claim 13 is not patent eligible under 35 U.S.C. § 101. Broadcom and Apple's briefing on this issue was cursory and relied solely on an argument that claim 13 is ineligible because it depends on mathematical operations. Caltech contends that the '781 patent is directed to a patent-eligible method of performing error correction and detection encoding with the requirement of irregular repetition. It asserts that the claim

limitation "variable number of subsets" requires irregular information bit repetition.

The mere fact that Caltech's claim employs a mathematical formula does not demonstrate that it is patent ineligible. *See Diamond v. Diehr*, 450 U.S. 175, 187 (1981) ("[A] claim drawn to subject matter otherwise statutory does not become nonstatutory simply because it uses a mathematical formula, computer program, or digital computer."). Claim 13 does not claim a mathematical formula as such. It claims more than a mathematical formula because it is directed to an efficient, improved method of encoding data that relies in part on irregular repetition. This alleged improvement is not patent ineligible simply because it employs a mathematical formula.

2. Infringement

Broadcom and Apple argue that even if claim 13 is directed to patent eligible subject matter, the infringement verdict as to claim 13 cannot stand. As discussed above, the parties agree that claim 13 requires irregular repetition, but dispute whether the district court erred in refusing to instruct the jury that the '781 patent's "variable number of subsets" limitation requires irregular repetition. The district court's sole ground for refusing to instruct the jury of the interpretation the parties and the court reached during summary judgment was to avoid "confus[ing] the record on this issue." J. App'x 207. This was error and requires remand for a new trial on infringement. *Sulzer Textil A.G. v. Picanol N.V.*, 358 F.3d 1356, 1366 (Fed. Cir. 2004) ("[I]t is the duty of trial courts in patent cases in which claim construction rulings on disputed claim terms are made . . . to inform jurors both of the court's claim construction rulings on all disputed claim terms and of the jury's obligation to adopt and apply the court's determined meanings[.]"). On remand, the district court must instruct the jury as to the proper construction of the claim limitation "variable number of subsets."

III. Validity and IPR Estoppel

Apple and Broadcom contend that the district court erred in granting summary judgment of no invalidity, barring them from presenting an invalidity case at trial on the ground of statutory estoppel. In the district court proceedings, the parties challenged the patents' invalidity, relying on grounds the PTAB did not address in its earlier instituted IPR decisions. The district court nonetheless held that these challenges were barred by estoppel because Apple and Broadcom were aware of the prior art references at the time they filed their IPR petitions and reasonably could have raised them in those petitions even if they could not have been raised in the proceedings post-institution.

Before the district court, Broadcom and Apple brought counterclaims seeking declaratory judgment of invalidity under § 103. The district court's summary judgment orders disposed of the parties' affirmative defenses as well as their counterclaims. We therefore consider whether this ruling was erroneous and review the grant of summary judgment de novo. *Synopsys, Inc. v. Mentor Graphics Corp.*, 839 F.3d 1138, 1146 (Fed. Cir. 2016).

When IPR proceedings result in a final written decision, 35 U.S.C. § 315(e)(2) precludes petitioners from raising invalidity grounds in a civil action that they "raised or reasonably could have raised *during* that inter partes review." *Shaw Industries Group, Inc. v. Automated Creel Systems, Inc.*, 817 F.3d 1293, 1300 (Fed. Cir. 2016) (emphasis added). In *Shaw*, this court held that IPR "does not begin until it is instituted." *Id.* If IPR "does not begin until it is instituted," grounds raised in a petition (or that reasonably could have been raised in a petition) were necessarily not raised "*during* the IPR." *Id.* Only the grounds actually at issue in the IPR were raised, or reasonably could have been raised in the IPR. Thus, estoppel did not bar the petitioner in *Shaw* from presenting a petitioned-

for, non-instituted ground in future proceedings because the petitioner could not reasonably have raised the ground during IPR. *Id.* *Shaw* was followed in *HP Inc. v. MPHJ Technology Investments, LLC*, 817 F.3d 1339, 1347–48 (Fed. Cir. 2016). At the time *Shaw* was decided, the PTAB often instituted review on less than all the grounds raised in a petition, which left some grounds unadjudicated on the merits. Before *Shaw*, we had held in *Synopsys, Inc v. Mentor Graphics Corp.*, 814 F.3d 1309, 1314–15 (Fed. Cir. 2016), that the PTAB's final decision need not address every claim raised in a petition. Under such circumstances, we concluded that Congress could not have intended to bar later litigation of the issues that the PTAB declined to consider.

After *Shaw*, several district courts concluded that *Shaw* does not allow a petitioner to avoid estoppel as to all arguments that could have been raised in the petition. *See, e.g.*, *SiOnyx, LLC v. Hamamatsu Photonics K.K.*, 330 F. Supp. 3d 574, 602 (D. Mass. 2018) (determining that estoppel applies to grounds not included in a petition that the petitioner reasonably could have raised); *Cobalt Boats, LLC v. Sea Ray Boats, Inc.*, Case No. 15-cv-21, 2017 WL 2605977, at *3 (E.D. Va. June 5, 2017) (same); *Biscotti Inc. v. Microsoft Corp.*, Case No. 13-cv-1015, 2017 WL 2526231, at *7 (E.D. Tex. May 11, 2017) (same); *Douglas Dynamics, LLC v. Meyer Prods. LLC*, Case No. 14-cv-886, 2017 WL 1382556, at *5 (W.D. Wis. Apr. 18, 2017) (same); *Parallel Networks Licensing, LLC v. IBM Corp.*, Case No. 13-cv-2072, 2017 WL 1045912, at *12 (D. Del. Feb. 22, 2017) (same); *Oil-Dri Corp. of Am. v. Nestle Purina Petcare Co.*, Case No. 15-cv-1067, 2017 WL 3278915, at *8 (N.D. Ill. Aug. 2, 2017) ("[W]hile it makes sense that noninstituted grounds do not give rise to estoppel because a petitioner cannot—to no fault of its own—raise those grounds after the institution decision, when a petitioner simply does not

raise invalidity grounds it reasonably could have raised in an IPR petition, the situation is different.").

Other district courts read *Shaw* differently, focusing on *Shaw*'s discussion of the "during the IPR" language in § 315(e)(2). *See, e.g.*, *Koninklijke Philips N.V. v. Wangs All. Corp.*, Case No. 14-cv-12298, 2018 WL 283893, at *4 (D. Mass. Jan. 2, 2018) ("It would seem, then, that the phrase "inter partes review" . . . refers only to the period of time after review is instituted, and, therefore, the estoppel provision does not apply to arguments that the petitioner only 'raised or reasonably could have raised' in its petition rather than after institution of review."); *Verinata Health, Inc. v. Ariosa Diagnostics, Inc.*, Case No. 12-cv-5501, 2017 WL 235048, at *3 (N.D. Cal. Jan 19, 2017) ("The [*Shaw*] court chose instead to interpret the IPR estoppel language literally, plainly stating that only arguments raised or that reasonably could have been raised during IPR are subject to estoppel."); *Intellectual Ventures I LLC v. Toshiba Corp.*, 221 F. Supp. 3d 534, 553–54 (D. Del. 2016) (holding that although exempting nonpetitioned grounds from estoppel "confounds the very purpose of this parallel administrative proceeding, the court cannot divine a reasoned way around the Federal Circuit's interpretation in *Shaw*").

After *Shaw*, in *SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018), the Supreme Court made clear both that there is no partial institution authority conferred on the Board by the America Invents Act and that it is the petition, not the institution decision, that defines the scope of the IPR. *See id.* at 1357–58 ("[T]he statute tells us that the petitioner's contentions, not the Director's discretion, define the scope of the litigation . . . There is no room in this scheme for a wholly unmentioned 'partial institution' power that lets the Director select only some challenged claims for decision."). Given the statutory interpretation in *SAS*, any ground that could have been raised in a petition is a ground that could have been reasonably raised

"during inter partes review." Thus, the Supreme Court's later decision in *SAS* makes clear that *Shaw*, while perhaps correct at the time in light of our pre-*SAS* interpretation of the statute cannot be sustained under the Supreme Court's interpretation of related statutory provisions in *SAS*.

The panel here has the authority to overrule *Shaw* in light of *SAS*, without en banc action. To be sure, *SAS* did not explicitly overrule *Shaw* or address the scope of statutory estoppel under § 315(e)(2). But the reasoning of *Shaw* rests on the assumption that the Board need not institute on all grounds, an assumption that *SAS* rejected. Even in the Ninth Circuit, which has one of the stricter approaches to panel overruling, *see* Henry J. Dickman, *Conflicts of Precedent*, 106 Va. L. Rev. 1345, 1350–51 (2020), "the issues decided by the higher court need not be identical in order to be controlling. Rather, the relevant court of last resort must have undercut the theory or reasoning underlying the prior circuit precedent in such a way that the cases are clearly irreconcilable," *Miller v. Gammie*, 335 F.3d 889, 900 (9th Cir. 2003) (en banc). We approved that higher standard in *Troy v. Samson Manufacturing Corp.*, 758 F.3d 1322, 1326 (Fed. Cir. 2014), and conclude that that standard is satisfied in this case.

Accordingly, we take this opportunity to overrule *Shaw* and clarify that estoppel applies not just to claims and grounds asserted in the petition and instituted for consideration by the Board, but to all claims and grounds not in the IPR but which reasonably could have been included in the petition.[5] In a regime in which the Board must

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[5] In this case, *SAS* was decided while IPR proceedings remained pending before the Board. Accordingly, we need not decide the scope of preclusion in cases in which

institute on all grounds asserted and the petition defines the IPR litigation, this interpretation is the only plausible reading of "reasonably could have been raised" and "in the IPR" that gives any meaning to those words.

It is undisputed that Apple and Broadcom were aware of the prior art references that they sought to raise in the district court when Apple filed its IPR petitions. Despite not being included in any of Apple's IPR petitions, the contested grounds reasonably could have been included in the petitions, and thus in the IPR. We affirm the district court's decision barring Apple and Broadcom from raising invalidity challenges based on these prior art references.

IV. Inequitable Conduct

We turn next to the district court's grant of Caltech's summary judgment motion of no inequitable conduct. Generally, inequitable conduct requires a showing that undisclosed prior art was but-for material to the PTO's decision of patentability. *Therasense, Inc. v. Becton, Dickinson and Co.*, 649 F.3d 1276, 1291 (Fed. Cir. 2011). Prior art is but-for material if the PTO would have denied a claim had it known of the undisclosed prior art. *Id.* Prior art is not but-for material if it is merely cumulative. *Regeneron Pharms., Inc. v. Merus N.V.*, 864 F.3d 1343, 1350 (Fed. Cir. 2017) (citing *Dig. Control Inc. v. Charles Mach. Works*, 437 F.3d 1309, 1319 (Fed. Cir. 2006)).

Broadcom and Apple on appeal have limited their argument to the district court's conclusion that Richardson99 was not shown to be but-for material to patentability. The district court found that Richardson99 was merely cumulative of Luby97 and Luby98—references the PTAB considered in IPR proceedings upholding the patents' validity—

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the Board declined to institute on all grounds and issued its final written decision pre-*SAS*.

noting Apple and Broadcom's pleadings, interrogatory responses, and briefs failed to distinguish Luby's disclosed irregular repetition from Richardson99's. Apple and Broadcom did not argue at the summary judgment stage that Richardson99 was different from Luby such that it was not merely cumulative. The district court rejected the arguments as to Richardson99 because the Appellants failed to put Caltech on notice of an independent inequitable conduct theory based on alleged differences between Richardson99 and Luby.

The district court's decision was not an abuse of discretion. We therefore affirm the grant of summary judgment of no inequitable conduct.

V. Damages

Caltech presented to the jury a two-tier reasonable royalty model based on simultaneous hypothetical negotiations with Broadcom and Apple in December 2009. Broadcom and Apple generally argue that the damages judgement cannot be sustained because Caltech's damages model impermissibly applied two separate hypothetical negotiations for Broadcom and Apple for sales of the same chips; because Caltech's royalty rates were derived from non-comparable settlements—without apportionment and based on improperly excluded expert opinions and unrelated "black box" calculations; and because Caltech's damage model improperly included extraterritorial sales.

Caltech argues in response that the damages judgment properly rests on separate running-royalty rates for each defendant, that the district court's rulings on admissibility and exclusion of evidence were not an abuse of discretion and that the damages were based entirely on United States sales.

We find no error in the district court's jury instructions relating to extraterritoriality. But because Caltech's two-tier damages theory is legally unsupportable on this

record, the damages award is vacated and the case is remanded for a new trial on damages.

A. Extraterritoriality

Apple and Broadcom argue that the damages verdict improperly included extraterritorial sales from Broadcom's international affiliates. They argue that the district court erroneously instructed the jury on extraterritoriality for two reasons. First, they argue that the district court erroneously declined to instruct the jury of a presumption against extraterritorial application of United States laws. We see no error. The relevant presumption is whether a law applies extraterritorially. *See WesternGeco LLC v. ION Geophysical Corp.*, 138 S.Ct. 2129, 2134, 2136 (2018). But the dispute here is not whether infringement laws apply domestically or extraterritorially—there is no dispute that the laws apply only domestically. Rather, the dispute between the parties is whether the relevant transactions here were domestic or extraterritorial in nature. The presumption against extraterritorial application is thus inapplicable. As Caltech correctly argues, the district court expressly instructed the jury that Caltech had the burden of proving that infringement occurred in the United States. J. App'x 184–85 (instructing the jury that "An allaged infringer is liable for direct infringement of a claim if the patent holder proves by a preponderance of the evidence that the infringer, without the patent holder's authorization, imports, offers to sell, sells, or uses [the accused products] *within the United States*," and explaining the factors for determining whether a sale occurs in the United States). This was a proper and sufficient jury instruction with respect to the applicable burdens on the territoriality of the sales at issue.

Second, Apple and Broadcom argue that the district court erroneously instructed the jury that the "sales cycle leading to design wins" could trigger a United States sale. Apple and Broadcom argue that *Halo* recognized a

categorical prohibition against treating such a sales cycle as a domestic sale. *See Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 831 F.3d 1369, 1378 (Fed. Cir. 2016), *on remand from* 579 U.S. 93 (2016). *Halo* held that "pricing and contracting negotiations in the United States alone do not constitute or transform those extraterritorial activities into a sale within the United States for purposes of § 271(a)." *Id.* It held that this was so "when substantial activities of a sales transaction, including the final formation of a contract for sales encompassing all essential terms as well as the delivery and performance under that contract, occur entirely outside the United States." *Id.* This is not a blanket holding that design wins arising out of a sales cycle can never be domestic transactions. Indeed, the district court noted that a design win meeting these criteria, such that "substantial activities of a sales transaction . . . occurs entirely outside the United States" would *not* constitute a sale within the United States. J. App'x 185. The district court's jury instruction emphasized the key question of whether there were such substantial activities in the United States, an instruction that Apple and Broadcom do not contest. *See also Carnegie Mellon U. v. Marvell Tech. Grp., Ltd.*, 807 F.3d 1283, 1308 (Fed. Cir. 2015). There is no error in the district court's permissive instruction.

B. Caltech's Two-Tier Damage Model

Caltech presented its damage theory to the jury through two experts, Dr. Catherine Lawton and Dr. David Teece. They opined that Caltech would have engaged in two simultaneous hypothetical negotiations, one with Broadcom at the "chip level" and one with Apple at the "device level." Those negotiations would have excluded from Broadcom's hypothetical chip license any Broadcom chips incorporated into Apple products sold in the United States and treated those identical chips as being subject to Apple's separate hypothetical device license at a vastly different royalty rate. Both of Caltech's experts testified that separate chip-level and device-level negotiations would have

been proper, rather than a single hypothetical negotiation for all of the accused chips, because both defendants were separate infringers and there would be no "cross-talk" between them as they each engaged in their own hypothetical negotiation.

The district court considered the opinions of Caltech's experts and, over Broadcom and Apple's objection, permitted Caltech to present that theory to the jury. In doing so, the district court observed that "[p]atent owners will sometimes seek damages from accused infringers at different levels in the supply chain, and so long as they do not attempt to obtain a double recovery to violate other legal principles like patent exhaustion, they are free to do so." J. App'x 225. In ruling in Caltech's favor, the district court saw no concern over double recovery because Broadcom and Apple were different companies and because the experts' opinions carved out of the Broadcom hypothetical negotiation chips sold to Apple. But in the absence of some evidence that companies in the positions of Broadcom and Apple would engage in such separate negotiations and in the absence of additional facts that might justify separate and different treatment of the same chips at different levels of the supply chain, the mere fact that Broadcom and Apple are separate infringers alone does not support treating the same chips differently at different stages in the supply chain and does not justify submitting such a two-tier damage theory to the jury. It is generally recognized that in the usual case, "a direct infringer or someone who induced infringement should pay the same reasonable royalty based on a single hypothetical negotiation analysis." *LaserDynamics, Inc. v. Quanta Comput., Inc.*, 694 F.3d 51, 76 (Fed. Cir. 2012).

Caltech argued that separate royalty rates at different levels of the supply chain are proper because the reasonable royalty inquiry focuses on the amount of value that the patent technology adds to a product, citing *Ericsson, Inc. v.*

D-Link Sys., 773 F.3d 1201, 1226 (Fed. Cir. 2014). The district court concluded that Broadcom and Apple's products were different and therefore possessed different values simply because Broadcom and Apple were "different companies at different levels in the supply chain." J. App'x 226. But to reach that conclusion without more ignores established precedent to the effect that, in the absence of a compelling showing otherwise, a higher royalty is not available for the same device at a different point in the supply chain. As we previously held, "a reasonable royalty is not to be separately calculated against each successive infringer. Once full recovery is obtained from one infringer with respect to a particular infringing device, at most nominal additional damages may be awarded against another with respect to the same device." *Stickle v. Heublein, Inc.*, 716 F.2d 1550, 1562 (Fed. Cir. 1983). Moreover, "[a] party is precluded from suing to collect damages from direct infringement by a buyer and user of a product when actual damages covering that very use have already been collected from the maker and seller of that product." *Glenayre Elecs., Inc. v. Jackson*, 443 F.3d 851, 864 (Fed. Cir. 2006).

The district court cited but distinguished those cases as only applying to damages calculations against two defendants involving overlapping royalty bases, a situation not existing here based on Caltech's expert's exclusion of chips sold to Apple from the royalty base considered for Broadcom. But that exclusion in this case is wholly contrived, lacks any basis of fact and is contrary to the customary way patent infringement disputes are ordinarily resolved. It is well settled that a reasonable royalty is what a willing licensor and a willing licensee would have agreed to at a hypothetical negotiation just before infringement began. See *Carnegie Mellon Univ. v. Marvell Tech. Grp.*, 807 F.3d 1283, 1303-1304 (Fed. Cir. 2015). Here, there is nothing in the record to suggest that Broadcom and Apple would have been willing to negotiate in this artificial way rather than to more conventionally negotiate a single

license at a single rate for the same chips. Neither of Caltech's experts offered any factual basis to conclude that Broadcom and Apple would have been willing to engage in separate negotiations leading to vastly different royalty rates for the same chips. The district court's views to the contrary and its limiting of the *Stickle* and *Glenayre* cases to situations involving double recovery were misplaced and erroneous. Caltech's two-tier damages theory is legally unsupportable on this record.

* * *

We need not and do not address Broadcom and Apple's indemnification argument, or their argument that the hypothetical negotiations would have been held not with Caltech but by its exclusive licensee, Inforon. Nor do we address Broadcom and Apple's argument based on smallest-saleable-patent-practicing-unit, or the sufficiency of the evidence as to the domestic or extraterritorial character of Broadcom's sales.

CONCLUSION

For the foregoing reasons, we affirm the district court's construction of the claim limitation "repeat." We affirm the district court's denial of JMOL on infringement of the asserted claims of the '710 and '032 patents. We affirm the district court's conclusion that claim 13 of the '781 patent is patent-eligible but vacate the jury's verdict of infringement thereof and remand for a new trial. We affirm the district court's summary judgment findings of no invalidity based on IPR estoppel and no inequitable conduct. We affirm the district court's jury instructions relating to extraterritoriality, but vacate the jury's damage award and remand for a new trial on damages.

AFFIRMED IN PART, VACATED IN PART, AND REMANDED.

COSTS

Each party shall bear its own costs.

United States Court of Appeals for the Federal Circuit

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Plaintiff-Appellee

v.

BROADCOM LIMITED, NKA BROADCOM INC., BROADCOM CORPORATION, AVAGO TECHNOLOGIES LIMITED, NKA AVAGO TECHNOLOGIES INTERNATIONAL SALES PTE. LIMITED, APPLE INC.,
Defendants-Appellants

2020-2222, 2021-1527

Appeals from the United States District Court for the Central District of California in No. 2:16-cv-03714-GW-AGR, Judge George H. Wu.

DYK, *Circuit Judge*, concurring-in-part and dissenting-in-part.

While I join Discussion sections II.B.1, III, and IV of the majority opinion, I respectfully disagree with the majority's holding that substantial evidence supports the jury's verdict of infringement of the asserted claims of the '710 and '032 patents and would reverse the district court's denial of JMOL of no literal infringement. I would similarly reverse the denial of JMOL rather than remand for a

new trial with respect to the infringement of the '781 patent.

I

No matter how novel an invention is, it is the patent's claims that "determine what the invention is," as well as the bounds of the patent owner's rights to that invention's "exclusive use." *Motion Picture Patents Co. v. Universal Film Mfg. Co.*, 243 U.S. 502, 510 (1917). Patent owners are limited by the language in the claims, and "can claim nothing beyond them." *Id.* (quoting *Keystone Bridge Co. v. Phoenix Iron Co.*, 95 U.S. 274, 278 (1877)). It is the patent owner's burden to show that "the properly construed claim reads on the accused device exactly." *CommScope Techs. LLC v. Dali Wireless Inc.*, 10 F.4th 1289, 1295 (Fed. Cir. 2021) (quoting *Engel Indus., Inc. v. Lockformer Co.*, 96 F.3d 1398, 1405 (Fed. Cir. 1996)). Denial of JMOL of no literal infringement must be reversed when plaintiffs "fail[] to present evidence proving that the [accused device] meets the district court's construction of [a] claim term." *CommScope*, 10 F.4th at 1295. Such a failure occurs when expert testimony "points to the result . . . rather than the specific mechanism claimed to achieve that result," *id.* at 1297, or when expert testimony is merely "cursory," *Alexsam, Inc. v. IDT Corp.*, 715 F.3d 1336, 1341–42 (Fed. Cir. 2013). Here, no showing of literal infringement has been made that can support the jury's infringement verdict under the district court's claim construction, which is not challenged by Caltech.

II

Before trial, the district court held a *Markman* hearing to construe the term "repeat," an essential limitation in all of the asserted claims of the three patents. Caltech advocated for the term's plain and ordinary meaning. Apple and Broadcom proposed a narrower construction, contending that "repeat" should be construed as "creating a new bit that corresponds to the value of an original bit (i.e., a new

copy) by storing the new copied bit in memory. A reuse of a bit is not a repeat of a bit." J.A. 9. The district court rejected this construction because reusing bits by "selecting the bits for use without necessarily storing them at a specific location in computer memory" could satisfy the claim limitation. J.A. 10. The district court nonetheless noted that the "claim language . . . makes clear that 'repeated bits' are a construct distinct from the original bits from which they are created." *Id.* Ultimately, the district court adopted the term's plain and ordinary meaning, concluding that no further construction was required.

Following the *Markman* hearing, the parties continued to dispute what exactly the plain and ordinary meaning of "repeat" entailed. As a result, at trial, as permitted by precedent,[1] the district court revisited and clarified its earlier claim construction ruling, instructing the jury that the '710 and '032 patents' claimed repetition requires the "generation of additional bits, where generation can include, for example, duplication or reuse of bits." J.A. 171. The critical question, therefore, is whether there is substantial evidence that the accused devices cause "generation of additional bits." Unfortunately, in denying the appellants' post-trial JMOL motion, the district court provided no analysis of how Caltech established infringement, relegating this question to a footnote which said only that

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[1] It is within the district court's discretion to "engage in a rolling claim construction, in which the court revisits and alters its interpretation of the claim terms as its understanding of the technology evolves." *See, e.g.*, *Jack Guttman, Inc. v. Kopykake Enters.*, 302 F.3d 1352, 1361 (Fed. Cir. 2002) (citing *Sofamor Danek Grp., Inc. v. DePuy–Motech, Inc.*, 74 F.3d 1216, 1221 (Fed. Cir. 1996)); *CollegeNet, Inc v. ApplyYourself, Inc.*, 418 F.3d 1225, 1233–34 (Fed. Cir. 2005).

"Defendants' arguments that the verdict was not supported by substantial evidence also remain unpersuasive." J.A. 206.

The panel majority does not identify or rely on a reuse theory to uphold the jury's verdict. Rather, the majority concludes that infringement of the repeat limitation was supported by expert testimony that "the [AND] gate affirmatively enables the information bit to be duplicated as the output bit. That is a 'repeat' . . . because the information bit in that situation 'flows through' to appear again in the output." Maj. Op. at 16 (emphasis added). But there is in fact no such expert testimony. To the contrary—consistent with its claim construction position, Caltech's expert testified that the claims do not "require that the repeat has to be done by duplicating information bits," J.A. 2858, and Caltech argued to this court on appeal that "repetition does not require duplication," Appellee's Br. 18.

To be sure, Caltech is correct that duplication is not required to satisfy the repeat limitation. But the problem for Caltech (and for the majority) is that Caltech never established that the accused devices generate "additional bits," as required by the district court's claim construction. The infringement theory presented at trial explained that the accused devices work as follows: information bits are input into the accused devices, those bits travel down branched wires to the inputs of 972 AND gates, and three to twelve of those AND gates will be open for each information bit, thus outputting the bits a different number of times. For this theory to satisfy Caltech's burden, Caltech was required to establish where, when, and how additional bits were generated.

One possibility—presented by Caltech's counsel—was that additional bits were generated by branching at the inputs. During closing arguments, Caltech told the jury "That's how you repeat bits, with a voltage along wires . . . how else would you repeat bits? How else would you do it?"

1/28 Tr. 90:20–91:9. But the record does not support a theory that the branched wires generate additional bits. Caltech's experts testified merely that the bits are "connected to" the AND gates by branched wires, without explaining whether or how that connection generated additional bits. J.A. 2831. Apple and Broadcom presented unrefuted expert testimony that the branched wire connection involves simultaneously sending the same bit—not an additional bit—to the inputs of AND gates. Caltech's expert did not testify to the contrary, and in fact declined to testify that branching generates additional bits.

> Q. Branch wire creates repeat bits?
>
> . . .
>
> THE COURT: I'll allow him to answer the question if he understands it.
>
> THE WITNESS: That question I did not understand. I didn't think it was well formed.
>
> BY MR. MUELLER: Q. The branch wire in the Broadcom chips in your view creates repeat bits within the meaning of the claims; correct?
>
> . . .
>
> THE WITNESS: In my analysis the branch wire is being used in conjunction with the tables and these and gates to implement irregular repetition.

J.A. 3019–20. There is no substantial evidence supporting an infringement verdict based on branching.

Caltech's separate theory to establish that the accused devices generate additional bits was the "flow through" theory, supported, according to the majority, by expert testimony that "the information bit 'flows through' to the output gate [when] the parity-check bit is 1," and that the flow through bit constitutes "a repeat, both according to the expert's usage and a plain understanding of the word." Maj.

Op. at 16–17. The majority identifies record evidence where Caltech's expert summarily testified that the AND gates repeated information bits when the gates are enabled, J.A. 2842; J.A. 3080, and where the expert concluded that the AND gates were "generating additional bits at their output," J.A. 4162. This cursory and conclusory testimony cannot satisfy Caltech's burden.

Caltech's own expert testimony as to how an AND gate functions forecloses concluding that the AND gates generate additional bits. Throughout trial, Caltech's expert consistently testified that an AND gate "act[s] like a switch . . . allowing the information bits to flow through . . . or not." J.A. 3016–17; *see also* J.A. 3031 ("[E]nable one allows the AND gate to act like a switch. So enable would close the switch and allow the one to come out."); J.A. 3030 ("[T]he AND gate has two inputs. One of them is the enable that allows the switch to open or close."); J.A. 3031 ("Enable zero is like the switch not allowing the information bit to flow through."). If an enabled AND gate merely allows the same information bit that already exists at the input of an AND gate "to come out," J.A. 3031, or to "flow through," this does not remotely establish how the AND gate output generates additional information bits. Under the explanation that Caltech repeatedly presented, one information bit comes in and one information bit comes out—no additional bit appears anywhere. Flow through, with a 1:1 ratio of input bits to output bits as described by Caltech's experts, cannot satisfy the generation of additional bits limitation required by the district court's claim construction.

Caltech's remaining theory submits that the accused devices generate additional bits when the branched wires are combined with the AND gates. The majority believes that "the physical connection of the first inputs of all 972 AND gates . . . *and* the connection of the parity-bit system to the other inputs of the AND gates to selectively enable 3 to 12 of those gates . . . *together* implement irregular repetition." Maj. Op. at 17. Neither the majority's opinion,

Caltech's briefs, and most importantly, Caltech's experts, explain why the combination of these two non-infringing components results in infringement. The district court therefore erred in denying JMOL of no literal infringement.

III

At trial, Caltech also presented a doctrine of equivalents case to the jury. In a footnote to its JMOL decision, the district court found that it was "not necessary" to analyze Apple and Broadcom's challenge to the doctrine of equivalents arguments, J.A. 206, and the majority here similarly does not address such a theory. There is no basis to sustain the verdict on a doctrine of equivalents theory.

To prevail, Caltech had the burden of proving equivalence "between the elements of the accused product or process and the claimed elements of the patented invention," *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 21 (1997), by showing that "the accused device contains an element that is not 'substantially different' from any claim element that is literally lacking," *Kraft Foods, Inc. v. Int'l Trading Co.*, 203 F.3d 1362, 1371 (Fed. Cir. 2000) (citing *Warner-Jenkinson*, 520 U.S. at 40).

Caltech's appellate brief devoted only one and a half pages to this issue, citing to eight pages of trial testimony in which its expert asserted that the differences between the accused chips and the claim limitations were insubstantial. At trial, Dr. Shoemake testified that because the claims do not "require repeating with any type of specific circuitry," any differences in the method Broadcom's chips used to accomplish the "overall goal" of the claims were insubstantial. J.A. 2856–58.

But even if no specific circuitry is required, Dr. Shoemake never explained why a bit flowing through to the output of an AND gate is substantially similar to the claimed device that generates additional bits. This is reminiscent

of the insufficient, "[g]eneralized testimony" proscribed by *Texas Instruments Inc. v. Cypress Semiconductor Corp.*, 90 F.3d 1558, 1567 (Fed. Cir. 1996), and it cannot satisfy Caltech's burden to provide "particularized testimony and linking argument as to the 'insubstantiality of the differences' between the claimed invention and the accused device or process . . . on a limitation-by-limitation basis," *id.* There was no basis for the jury to find infringement under the doctrine of equivalents.

I would reverse the district court's denial of JMOL and enter judgment of non-infringement for Broadcom and Apple.