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Paper 7
Date: March 16, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

VOLKSWAGEN GROUP OF AMERICA, INC.,
Petitioner,

v.

ARIGNA TECHNOLOGY LTD.,
Patent Owner.

IPR2021-01531
Patent 8,289,082 B2

Before GARTH D. BAER, SHARON FENICK, and IFTIKHAR AHMED, *Administrative Patent Judges*.

FENICK, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Volkswagen Group of America, Inc. ("Petitioner") filed a Petition (Paper 2, "Pet."), requesting an *inter partes* review of claims 1–32 of U.S. Patent No. 8,289,082 B2 (Ex. 1001, "the '082 Patent"). Arigna Technology Ltd. ("Patent Owner") filed a Preliminary Response to the Petition (Paper 6, "Prelim. Resp.").

We have authority under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a) to determine whether to institute *inter partes* review. For the reasons that follow, we institute an *inter partes* review as to the challenged claims of the '082 patent.

II. BACKGROUND

A. Real Parties In Interest

Petitioner identifies itself, Volkswagen AG; Audi AG; Bentley Motors Limited; and Automobili Lamborghini S.p.A. as real parties in interest. Pet. 81. Patent Owner identifies only itself as a real party in interest. Paper 5 (Patent Owner Mandatory Notices), 2.

B. Related Matters

The '867 patent is at issue in *Arigna Technology Limited v. Volkswagen AG et al.*, Case No. 2:21-cv-00054-JRG-RSP (E.D. Tex.) and ITC Proceeding 337-TA-1267 ("ITC proceeding"). Pet. 81; Paper 5, 2.

C. The '082 Patent

The '082 patent is directed to the adjustment of an offset of an output current of a current amplifier. Ex. 1001, code (54). The '082 patent explains that a current amplifier takes as input an input current and outputs a current output, which is intended to be I_O, the input current amplified by the current amplification of the current amplifier, but may include an offset

current I_{off}, which is an undesirable offset that can be positive or negative in regard to the current direction. *Id.* at 1:29–31, 5:32–44. To address the undesirable offset, an adjusting circuit is provided, which, in the ideal case, subtracts the offset. *Id.* at 1:45–49. Figure 2a, reproduced below, is a circuit diagram of an exemplary embodiment of a current amplifier and an adjusting circuit. *Id.* at 5:24–25, 5:50–55.

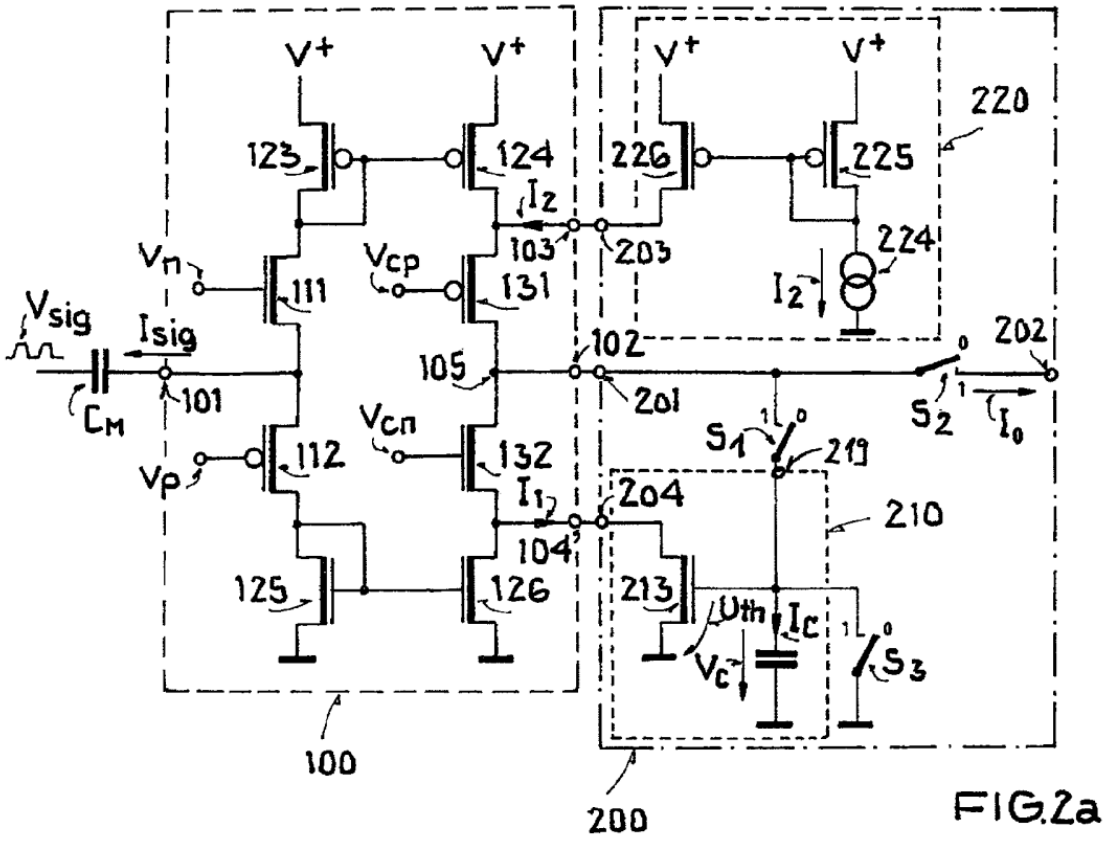


Figure 2a depicts input circuit amplifier 100 including a first current mirror with a first transformation ratio made up of PMOS transistors 123 and 124. *Id.* at 5:55–57. NMOS transistors 125 and 126 form a second current mirror with a second transformation ratio. *Id.* at 5:58–60. The first current mirror is connected to supply voltage V+ and the second current mirror to ground. *Id.* at 5:57–58, 5:60–61. When the first transformation ratio and the second

transformation ratio are not the same, an offset I_{off} will appear at the current output of current amplifier 100. Output transistor 124 of the first current mirror is connected to current summing node 105 via PMOS transistor 131; output transistor 126 of the second current mirror is connected to current summing node 105 via NMOS transistor 132. *Id.* at 6:6–11.

Also depicted in Figure 2a is adjusting circuit 200, formed to adjust the offset I_{off} to a minimum, preferably to zero. *Id.* at 6:15–19. Adjusting circuit 200 includes two current sources, controlled current source 210 and constant current source 200.

Controlled current source 210 generates a controlled current I_1 at its output. *Id.* at 6:42–43. In the embodiment of Figure 2a, controlled current source 210 is connected to NMMOS output transistor 126 of the second current mirror in input current amplifier 100, so the output of that output transistor and the output current I_1 of controlled current source 210 are summed. *Id.* at 6:43–52; *see id.* at 1:44–45, 3:60–4:3. In other embodiments, controlled current source is connected to output 102 of input amplifier 100. *Id.* at 6:52–54; *see id.* at 1:44–45, 3:60–4:3. Generally the Specification describes that the output I_1 of the controlled current source has an opposite current direction than the output of the current amplifier and is "connected to the current amplifier for impressing the output current of the controlled current source in the current amplifier." *Id.* at 1:41–43; *see id.* at code (57), 3:23–34, 3:65–4:3, 7:39–41. In other embodiments, controlled current source is connected to current input 101 of current amplifier 100. *Id.* at 1:45–47, 3:35–40, 7:20–23, 7:24–27, 7:31–35.

Constant current source 220 generates a constant current I_2, which is, in the embodiment of Figure 2a, connected to PMOS output transistor 124 of

the first current mirror, so the output current of output transistor 124 is summed with the output of constant current source 220, and connected to output 102 of current amplifier 102. *Id.* at 6:24–41.

D. Challenged Claims

Petitioner challenges claims 1–32. Of these, claims 1 and 17 are independent. Claims 1, 8, 9, and 17 are reproduced below with bracketed notations inserted for reference, corresponding to notations used in the Petition.

> 1. A circuit comprising:
>
> [1a] a current amplifier; and
>
> [1b] an adjusting circuit configured to correct an offset of an output current of the current amplifier, [1c] the adjusting circuit having a controlled current source and a first switching device,
>
> [1d] wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier,
>
> [1e] wherein an input of the controlled current source is connectable by the first switching device of the adjusting circuit to an output of the current amplifier to form a regulation element of a control loop,
>
> [1f] wherein the input of the controlled current source is disconnected from the output of the current amplifier by the first switching device to form a holding element,
>
> [1g] wherein the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current, and
>
> [1h] wherein the controlled current source, acting as a holding element, is configured to hold the current value, associated with the minimum, of the output current.

8. The circuit according to claim 1, wherein the adjusting circuit has a constant current source, which is connected to the current amplifier for producing a constant current.

9. The circuit according to claim 8, [9a] wherein the current amplifier has a current summing node that is connectable to the output of the current amplifier, [9b] wherein at least one first current and one second current are summed in the current summing node, [9c] wherein the first current is the output current of the controlled current source or is based on the output current of the controlled current source, and [9d] wherein the second current is the constant current of the constant current source or is based on the constant current of the constant current source.

17. A method for correcting an offset of an output current of a current amplifier of a circuit, the method comprising:

[17a] connecting a controlled current source to an output of the current amplifier via a first switching device, to form a regulation element of a control loop;

[17b] regulating an offset to a minimum by setting a current value of the output current of the controlled current source when an input signal of the current amplifier has a constant value, the controlled current source acting as the regulation element; and

[17c] disconnecting the controlled current source from the output of the current amplifier by the first switching device to form a holding element for holding the current value associated with the minimum of the output current.

Ex. 1001, 10:13–36, 10:58–11:3, 11:44–57.

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability. Pet. 2.

Reference(s)	Challenged Claims	35 U.S.C. §[1]
Soneda[2, 3]	1–6, 11, 13, 14, 16–22, 27, 29–32	§ 103
Soneda, Kozisek[4]	1–6, 8–11, 13, 14, 16–22, 24–27, 29–32	§ 103
Soneda, Palmisano[5]	7, 23	§ 103
Soneda, Kozisek, Palmisano	7, 23	§ 103
Soneda, Gutzki[6]	12, 15,[7] 28, 31	§ 103
Soneda, Kozisek, Gutzki	12, 15, 28, 31	§ 103

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 for applications filed on or after March 16, 2013. The '082 Patent issued in 2012. *See* Ex. 1001, code (45). Accordingly, for the purpose of institution, we apply the pre-AIA version of 35 U.S.C. § 103.

[2] Soneda, JP 62-171212, published July 28, 1986 (Ex. 1005, original at pp. 12–15, translation at pp. 2–11, affidavit of translator at p. 1 (*see* 37 C.F.R. § 42.63(b))).

[3] While the grounds chart provided by the Petitioner does not list grounds not including Kozisek, the arguments made encompass obviousness over Soneda alone. *See*, *e.g.*, Pet. 12–33 (using Kozisek only in the alternative in arguments relating to limitations 1e and 1g of claim 1). Arguments with respect to certain dependent claims rely solely on Kozisek in combination with Soneda. *See*, *e.g.*, Pet. 46–47 (arguing claims 8 and 24 based on obviousness over a combination of Soneda and Kozisek).

[4] Kozisek et al., US 6,049,246, issued Apr. 11, 2000 (Ex. 1006).

[5] Palmisano, G., Palumbo, G., & Pennisi, S., CMOS CURRENT AMPLIFIERS (1999) (Ex. 1007).

[6] Gutzki et al., US 7,405,614 B2, issued July 29, 2008 (Ex. 1008).

[7] While Petitioner's arguments for claims 15 and 31 appear in the discussion relating to obviousness over Soneda and Kozisek, these claims depend from claims 12 and 28 respectively, which are argued with reference to Soneda, Kozisek, and Gutzki. We assume this was a clerical error.

Petitioner also relies on a declaration from Laurence W. Nagel, Ph.D. (Ex. 1003).

III. DISCRETIONARY DENIAL UNDER 35 U.S.C. § 314(a)

Patent Owner contends the Board should deny the Petition under § 314(a) "[g]iven the advanced state of the [parallel] ITC Proceeding—which addresses the same issues raised in the instant Petition." Prelim. Resp. 44. For the reasons that follow, we decline to exercise our discretion to deny the Petition on that basis.

The Board's precedential decision in *Apple Inc. v. Fintiv Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"), identifies a non-exclusive list of factors parties may consider addressing where there is a related, parallel district court action to determine whether such action provides any basis for discretionary denial. *Fintiv*, Paper 11 at 5–16. Those factors include:

> 1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
>
> 2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
>
> 3. investment in the parallel proceeding by the court and the parties;
>
> 4. overlap between issues raised in the petition and in the parallel proceeding;
>
> 5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
>
> 6. other circumstances that impact the Board's exercise of discretion, including the merits.

Id. at 5–6.

In evaluating the factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Id.* at 6.

1. Factor 1

Neither party has sought a stay in the ITC proceeding. Pet. 7; Prelim. Resp. 46. We do not speculate about the likelihood of one. This factor is neutral.

2. Factor 2

The ITC proceeding has a November 28, 2022 target date for completion, which is approximately four months before the deadline for a final written decision in this proceeding. Pet. 7; Prelim. Resp. 46–47; Ex. 2004, 4.

Given the proximity between the projected ITC proceeding's completion date and the final written decision due date, on balance this factor weighs in favor of exercising our discretion to deny the Petition.

3. Factor 3

Patent Owner argues that there has been significant investment in the ITC Proceeding because "[t]he parties have already filed their *Markman* briefs and notices of prior art," and by the time this institution decision issues, "fact and expert discovery will be complete, and the summary judgment deadline will have passed." Prelim. Resp. 47. Petitioner notes its diligence in pursuing its petition and asserts the ITC investigation is in its early stage. Pet. 7. In these circumstances, we find this factor neutral.

4. Factor 4

As Petitioner notes, the issues in this case are somewhat different than the parallel ITC proceeding because only 13 of the 32 challenged claims in

this Petition are also at issue in the ITC proceeding. Pet. 7–8. Patent Owner argues that all the independent claims are challenged in the parallel ITC proceeding, and notes that the prior art used in the Petition is included in the documents identified in the Notice of Prior Art in the ITC proceeding. Prelim. Resp. 48; *see* Ex. 2006, 3–8 (Respondents' Joint Notice of Prior Art in the parallel ITC proceeding including Soneda, Kozisek, Palmisano, and Gutzki among approximately ninety prior art documents identified with respect to the '082 patent).

We agree with Petitioner that the additional claims at issue here, but not in the ITC proceeding, weigh against exercising our discretion to deny institution. While we acknowledge that Patent Owner has shown that the same references used here have been identified in the ITC proceeding, at this point in the proceeding it is not shown how or whether these references will be relied upon at trial. Thus, we determine this factor weighs against exercising our discretion to deny institution.

5. Factor 5

Neither party disputes that Petitioner and Patent Owner are parties to the ITC proceeding. Pet. 8; Prelim. Resp. 48. This factor favors exercising our discretion to deny institution.

6. Factor 6

Patent Owner contends "the merits of this Petition are weak." Prelim. Resp. 48. Petitioner argues that "[t]he merits are exceptionally strong." Pet. 8. As outlined below, we determine that the merits of the Petition meet the standard for institution of *inter partes* review. However, there are a number of factual disputes to be resolved at trial. Thus, while we determine that the merits meet the standard for institution of *inter partes* review, we do not

agree with either party that they are either particularly strong or weak. Thus, we find that this factor is neutral.

7. Summary and Conclusion

We have considered the circumstances and facts before us in view of the *Fintiv* factors. For the reasons given, we are not persuaded to exercise our discretion to deny institution.

IV. OBVIOUSNESS ANALYSIS

A. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech. Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc*., 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner must explain with particularity how the prior art would have rendered the challenged claims unpatentable. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104 ("The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.").

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. See *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.[8] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Skill in the Art

Petitioner contends a person of ordinary skill in the art "would have had a minimum of a Master's degree in electrical engineering or a similar field, and approximately two years of industry or academic experience designing or analyzing electronic circuits," where "[a]dditional education could substitute for professional experience, and significant work experience could substitute for formal education." Pet. 6 (citing Ex. 1003 ¶ 50). Patent Owner quotes but does not substantively comment on Petitioner's proposed definition, or offer an alternative definition. Prelim. Resp. 18.

Petitioner's description is consistent with the prior art and patent specification before us and is supported by credible expert testimony. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). For the purpose of this decision, we adopt Petitioner's description.

[8] Neither the Petition nor the Preliminary Response presents evidence or argument on the fourth *Graham* factor. We therefore do not consider that factor in this decision.

C. Claim Construction

In an *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2021). We apply the claim construction standard as set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc).

Claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and even extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

Neither party proposes any claim terms for construction. Pet. 6; Prelim. Resp. 24. We note, however, that while neither party expressly argues for a construction of limitation 1d of claim 1, the parties' arguments highlight a possible conflict in the construction of this claim limitation. Limitation 1d specifies that in the circuit of claim 1, "an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier." Ex. 1001, 10:19–22.

Petitioner, in its arguments with respect to the unpatentability of claim 1, implicitly argues that this term encompasses a situation in which an output current is generated in the controlled current source and this output current is connected to an output of the current amplifier. Pet. 16–20.

Patent Owner, in its arguments regarding Petitioner's assertions relating to limitation 1d, argues, at least implicitly, that this limitation does not encompass situations in which a controlled current source output is produced solely within the controlled current source, as opposed to being also produced within the current amplifier, through the connection of the controlled current source to a component of the current amplifier, such as NMOS transistor 132 of adjusting circuit 200 as shown in Figure 2a of the '082 patent. Prelim. Resp. 21, 25–30; Ex. 1001, 6:43–52.

We first turn to the intrinsic evidence to preliminarily determine the correct meaning for this limitation. The specification of the '082 patent describes a variety of configurations by which the controlled current source and the current amplifier may be connected. In one configuration, the controlled current source is connected to an input of the current amplifier. Ex. 1001, 1:45–47, 3:35–40, 7:20–23. In another configuration, the controlled current source is connected to an output of the current amplifier. *Id.* at 1:44–45, 2:19–21, 3:23–35, 6:19–23, 6:43–47. The controlled current source can be connected to the output of the current amplifier directly or via a component, such as a field-effect transistor. *Id.* at 3:62–64.

The claim language "producing an output current of the controlled current source in the current amplifier" does not appear in the specification. However, the specification describes "an output of the controlled current source" being "connected to the current amplifier for *impressing* an output current of the controlled current source in the current amplifier" in several places. *Id.* code (57), 1:41–43, 3:23–27, 7:39–41. We note specifically that the specification describes that this "impressing" may occur either by

connecting the controlled current source to an output of the current amplifier or to an input of the current amplifier. *Id.* at 1:44–47, 3:30–40.

The "impressing [of] an output current of the controlled current source in the current amplifier" in the specification corresponds to the claim language as originally filed. Ex. 1002, 123 (originally filed claim 1 reciting that "an output of the controlled current source is connectable to the current amplifier for *impressing* an output current of the controlled current source in the current amplifier" (emphasis added)). During prosecution, the Examiner objected to the term "impressing" and suggested the substitution of "producing." *Id.* at 51. This change was accepted by the applicant, who adopted it by amending the claims as suggested, and argued that the change was made to expedite issuance and were not narrowing or necessary for patentability. *Id.* at 32, 39.

In the sections of the specification describing "impressing" of the output of the controlled current source in the current amplifier, embodiments are discussed other than those where the connection of the output of the controlled current source output is to an internal component of the current amplifier. For the purposes of institution, we decline to read the claim as only applying to the embodiment in which the output is connected in this way without an indication in the record that the patentee intended the claims to be limited to that embodiment. *Liebel–Flarsheim v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed.Cir. 2004) ("[I]t is improper to read limitations from a preferred embodiment described in the specification . . . into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited.")

Based on this intrinsic record, we preliminarily determine that this limitation does not require the connection of the output of the controlled current source to an internal component (such as a transistor) of the current amplifier in such a way that production of an output current by the controlled current source occurs in some way in the current amplifier. For the purposes of institution, therefore, we do not adopt Patent Owner's narrower view of limitation 1d, but determine that the correct interpretation of limitation 1d encompasses circuits in which the output current of the controlled current source is impressed in the current amplifier. As we herein institute, the parties will have the opportunity to present additional argument and evidence regarding this preliminary determination.

Beyond this, we need not explicitly construe any terms to determine whether to institute an *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("we need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). We note, however, that a possible claim construction issue also exists with respect to limitation 9a of claim 9, as discussed below in Section IV.D.4.b.

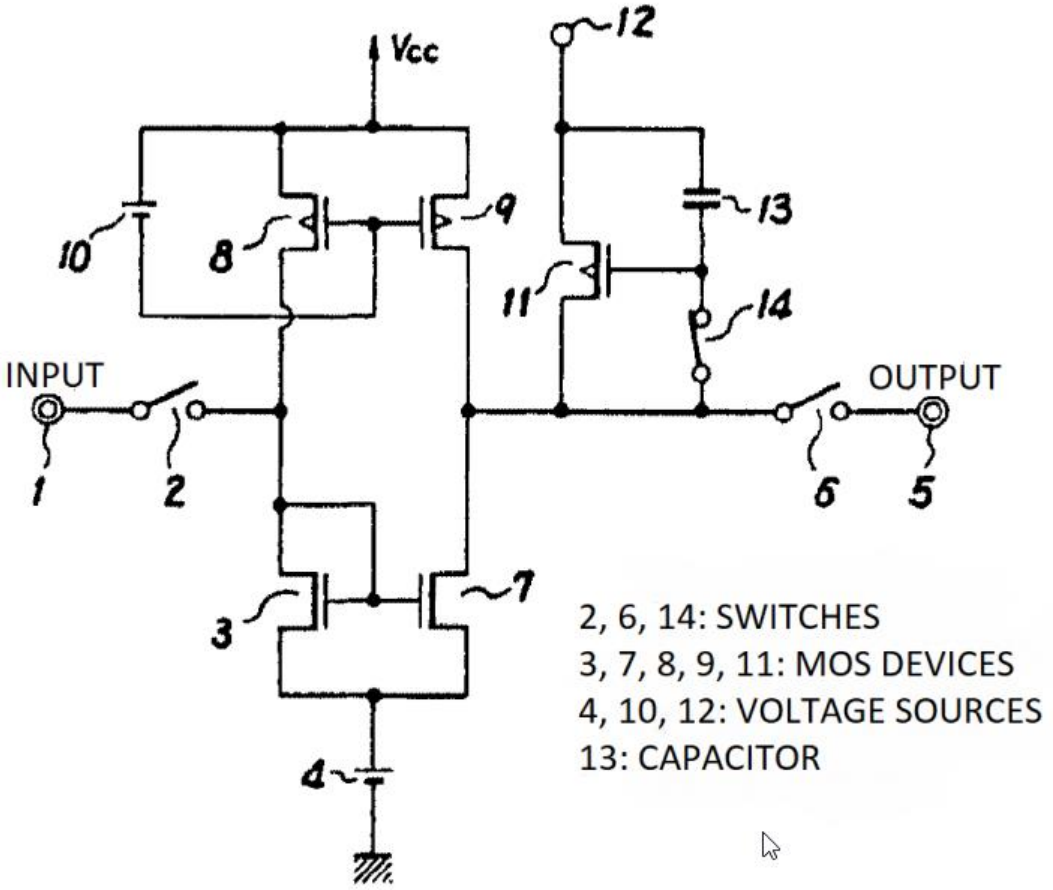
D. Claims 1–6, 8–11, 13–22, 24–27, and 29–32

Petitioner argues that claims 1–6, 11, 13, 14, 16–22, 27, 29–32 would have been obvious over Soneda and that claims 1–6, 8–11, 13–22, 24–27, and 29–32 would have been obvious over a combination of Soneda and Kozisek. Pet. 9–71. Patent Owner presents arguments relating to certain of these contentions. Prelim. Resp. 25–43. For the reasons discussed below, we determine that Petitioner has shown a reasonable likelihood that the

Petitioner would prevail with respect to claims 1–6, 8, 11, 13–22, 24–27, and 29–32.

1. Soneda

Soneda describes a current circuit that includes a current amplifier. Ex. 1005, 57–58, Fig. 5. Soneda provides a circuit in which an offset current of the current amplified is eliminated. *Id.* at 58–59. Soneda's Figure 1, reproduced below, illustrates a current amplifier in a circuit that allows for an output to be unaffected by offset current.



CONNECTION DIAGRAM OF WORKING EXAMPLE
FIG. 1

The example of Figure 1 includes current amplifier circuitry, including elements 3, 4, and 7–10. *Id.* at 58–59; *see id.* at 57, Fig. 5.

Additionally, the example of Figure 1 includes P-type MOS device 11, voltage source 12, capacitor 13, and switch 14, such that a current equal to the offset current is supplied from P-type MOS device 11. *Id.* at 58–59. "[A]ccording to this circuit, a current that is equal to the offset current . . . is supplied from the device (11) . . . and thereby an output-signal current can be obtained at the output terminal (5) that is unaffected by the offset current." *Id.* at 59.

2. Kozisek

Kozisek describes an adjusting circuit for use with a differential amplifier to correct for an offset current. Ex. 1003, code (57), 1:5–10. This circuit supplies an offset current having a magnitude equal and opposite to the output offset current of an amplifier. *Id.* at 5:52–54. Figure 2, reproduced below, is a schematic drawing of a circuit including a differential amplifier and circuitry to supply an offset cancellation current to the output of that differential amplifier. *Id.* at 4:20–23, 5:27–37.

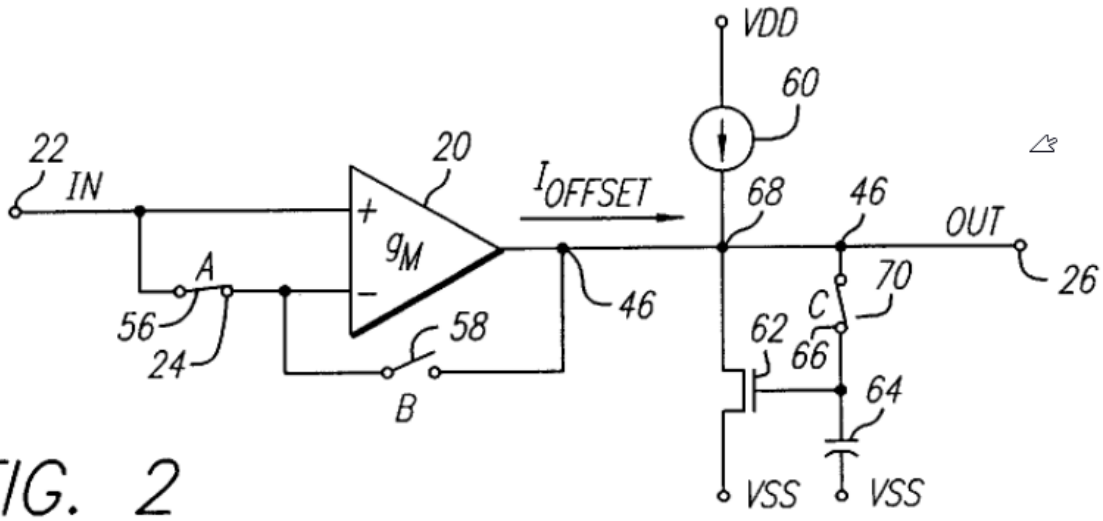


FIG. 2

In Figure 2, amplifier 20 has an output including a current offset, and a current copier circuit including current source 60, transistor 62, and storage

capacitor 66 functions to source current or sink current in order to offset that offset current. *Id.* at 5:52–63. Current source 60 sources a fixed amount of current. *Id.* at 6:1. Transistor 62 is biased to sink an amount of current which is greater than, less than, or equal to the amount of current sourced by current source 60, in order to eliminate the current offset. *Id.* at 5:30–37, 6:6-10, 6:22-29. The degree to which transistor 62 conducts current is controlled by storage capacitor 62. *Id.* at 6:6–10.

In a first phase, which Kozisek terms "cancellation mode" or "programming mode," first switch 56 is closed to null the input to the amplifier 20, second switch 58 is opened to disconnect the feedback loop, and third switch 70 is closed to allow the current copier circuit to sense and null out any output current offset at output node 46. *Id.* at 6:16–22, 6:38–39. In this way, the voltage at noted 46 and thus at first terminal 66, will drift until transistor 62 is biased to supply a current (along with current source 60) exactly balances any output offset current from amplifier 20. *Id.* at 6:23–31.

After this mode is performed, circuitry is switched to the normal mode of operation by opening third switch 70, opening first switch 56, and closing second switch 58. *Id.* at 6:39–43. The normal operation of amplifier 20 can occur, and the offset cancellation current set in the prior mode continues to be supplied by transistor 62 and the rest of the current copier circuitry. *Id.* at 6:12–15, 6:47–53.

3. Claim 1

Petitioner argues that claim 1 would have been obvious over Soneda and Kozisek. Pet. 12–33. Patent Owner presents arguments relating to these contentions. Prelim. Resp. 25–30, 38–42.

a. Preamble and Limitations 1a, 1b, and 1c of Claim 1

Petitioner argues that Soneda teaches or suggests the preamble and the first three limitations of claim 1. Petitioner argues that Soneda's Figure 1 teaches a circuit, and that the circuit comprises a current amplifier as described with reference to Figure 5. Pet. 12–14 (citing Ex. 1005, 57–58, Figs. 1, 5; Ex. 1003 ¶¶ 64–66). Petitioner additionally argues that Soneda's circuit as shown in Figure 1 includes an adjusting circuit configured to correct an offset of an output current of the current amplifier in Soneda's circuitry that supplies a current equal to the offset current from Soneda's transistor 11, and including capacitor 13 and switch 14. *Id.* at 14–16 (citing Ex. 1005, 59, Fig. 1; Ex. 1003 ¶¶ 67–69). Petitioner further argues that transistor 11 and capacitor 13 teach as the "controlled current source" of limitation 1c, and that switch 14 teaches the "first switching device" of that limitation. *Id.* at 16 (citing Ex. 1003 ¶¶ 70–71).

Patent Owner does not dispute these contentions.

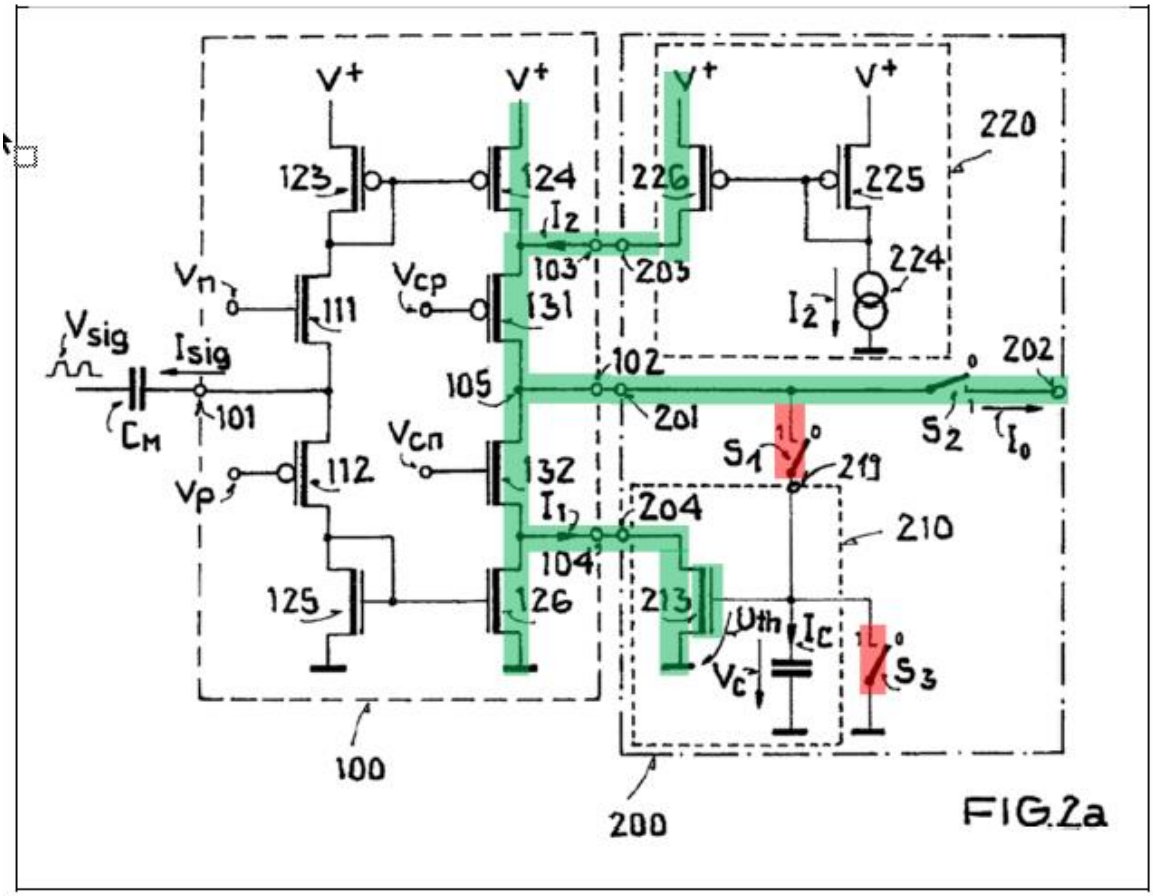
We determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests the subject matter of the preamble and limitations 1a, 1b, and 1c of claim 1.

b. Limitation 1d

Petitioner argues that limitation 1d, "wherein an output of the controlled current source is connectable to the current amplifier for producing an output current of the controlled current source in the current amplifier," is taught or suggested by Soneda. Pet. 19–20. Petitioner cites Soneda's disclosure that an offset current flows through device 11 and is supplied from device 11. *Id.* at 19 (citing Ex. 1005, 59, Fig. 1; Ex. 1003 ¶ 75). Petitioner additionally cites Soneda's teaching that the drain of device

11 "is connected to a connection midpoint between [MOS devices] (7) (9)." *Id.* (citing Ex. 1005, 58; Ex. 1003 ¶ 76).

Patent Owner asserts that Petitioner has failed to show that Soneda teaches or suggests "producing an output current of the controlled current source in the current amplifier." Prelim. Resp. 25–30. Patent Owner argues, with reference to Figure 2a of the '082 patent, that in that embodiment, the output current is produced "in the current amplifier itself, rather than solely in the separate adjusting circuit." *Id.* at 26–29. Patent Owner provides an annotated version of Figure 2a, reproduced below, in which it asserts "[t]his effect can be seen." *Id.*



It appears from Patent Owner's description of a prior figure that in this figure, "[e]xample flow of the relevant current at this stage is shown in green." *Id.* at 7, 14–16, 26–27.

Patent Owner asserts that, in contrast, Soneda does not show that an output current of the controlled current source would be produced in the current amplifier, but that it would only be produced in the adjusting circuit. Pet. 28–29. However, this argument appears to be based Patent Owner's implicit claim construction of "producing an output current of the controlled current source in the current amplifier" as discussed above in Section IV.C. Patent Owner's provided annotations in green of current flow in Figure 2a of the '082 Patent are instructive but do not address where current is "produced" or "impressed" in Figure 2, current flow in Soneda, or where in the Soneda circuit the output current of the device 11 would be impressed.

On the present record, we disagree with Patent Owner's assertion that Soneda does not teach or suggest limitation 1d. Soneda describes an adjusting circuit that supplies, via device 11, an offset current that flows between the source and drain of device 11. Ex. 1005, 59; Ex. 1003 ¶ 75. The drain of this device is connected to a connection midpoint between two devices *within* the current amplifier. Ex. 1005, 58; Ex. 1003 ¶ 76. On the record before us, Soneda teaches or suggests that the current supplied by device 11 is impressed in the current amplifier at a connection midpoint between devices 7 and 9. On the present record and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests limitation 1d.

c. Limitation 1e

i. Limitation 1e – Soneda

With respect to limitation 1e, Petitioner argues that Soneda teaches that the input of its adjusting circuit is connectable by a first switching device to the output of the current amplifier, which forms a regulation element of a control loop. Pet. 21–23. Petitioner argues that Soneda's switch 14 is turned on during a blanking interval, and connecting an input to the portion of the circuit identified as teaching the controlled current source to the output from the current amplifier. *Id.* at 21–22 (citing Ex. 1005, 58–59, Fig. 1; Ex. 1003 ¶ 78). During this time, Petitioner argues, the "controlled current source" acts as a regulation element of the control loop in regulating its current to be equal to the offset current of the current amplifier. *Id.* at 22–23 (citing Ex. 1005, 59; Ex. 1003 ¶¶ 80–81).

Patent Owner does not dispute Petitioner's contentions with respect to Soneda teaching or suggesting the subject matter of limitation 1e. We determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests the subject matter of limitation 1e.

ii. Limitation 1e – Soneda and Kozisek

Petitioner additionally argues that Kozisek teaches an adjusting circuit with a switching device for switching between a cancellation mode and a normal mode of operation. Pet. 23–24. Petitioner argues that first switching device 70 of Kozisek, when closed, is connected to an output of the amplifier 20 at terminal 46, and allows the voltage at the terminal 66 to "drift until the transistor 62 is biased in such a manner" that the net current supplied to terminal 68 balances the offset current that will be produced in

the amplifier. Pet. 23–24 (citing Ex. 1006, 5:52–54, 5:63–67, 6:6–10, 6:22–29, Fig. 2; Ex. 1003 ¶¶ 82–84).

Petitioner contends that one of ordinary skill would have combined Soneda and Kozisek's teachings, using Soneda's controlled current source as a regulation element of a control loop, having the capacitor 13 charged by offset current when first switching device 14 is closed, such that transistor 11 is biased to conduct current to balance the offset current. *Id.* at 25 (citing Ex. 1003 ¶ 86). Petitioner argues that this would have allowed Soneda to be used to operate with different values of offset current and to adapt to cancel offset regardless of the configuration, temperature, and noise of the current amplifier. *Id.* at 25–26. Petitioner further argues that one of ordinary skill would have had a reasonable expectation of success because of their similar structures, including a capacitor connected to an amplifier output for charging the capacitor during a regulating phase, and that one of ordinary skill would further have recognized that using Soneda's controlled current source as a regulation element would result in the expected current cancellation in Kozisek. *Id.* at 26–27 (citing Ex. 1003 ¶ 87).

Patent Owner argues that Petitioner has not identified why one of ordinary skill in the art would have modified Soneda based on Kozisek. Prelim. Resp. 38–41. Patent Owner argues that Petitioner identifies only surface similarities, and only offers hindsight-based suggestions of motivation, unsupported by more than declarant testimony. *Id.* Lastly, Patent Owner argues that Petitioner "lists general problems or goals regarding current amplifier offset calculation" but does not address why one of ordinary skill in the art would have looked to Kozisek to modify Soneda. *Id.* at 41.

On the present record and at this stage of the proceeding, Petitioner has adequately shown more than surface similarities between Kozisek and Soneda, each of which addresses the same problem with an adjusting circuit in which a capacitor is charged and provides a current used to balance the current amplifier's offset current. Pet. 9–12, 24–25. Additionally, we find sufficient Petitioner's declarant's uncontroverted testimony regarding motivation to combine in the discussion of Kozisek's circuit that allows a transistor to act to "exactly balance[]" the offset of an adjusting circuit effectively and flexibly. *Id.* at 24 (quoting Ex. 1006, 6:22–29), 26; Ex. 1003 ¶ 86. On the present record, and at this stage of the proceeding, Petitioner has shown sufficiently that the combination would have taught or suggested the claimed situation in which an adjusting circuit includes a switching device (Kozisek's first switching device 70) that connects an input of the controlled current source (input to transistor 62) to form a regulation element of a control loop.

Thus, we determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that the combination of Soneda and Kozisek teaches or suggests the subject matter of limitation 1e.

d. Limitation 1f of Claim 1

Petitioner argues that Soneda teaches or suggests the input of the controlled current source being disconnected from the output of the current amplifier by a switching device in Soneda's disclosure that, during an operation interval, switch 14 is turned off. Pet. 27–28 (citing Ex. 1005, 58–59; Ex. 1003 ¶ 89). Petitioner further argues that one of ordinary skill would understand from Soneda that when switch 14 is turned off, the controlled

current source acts as a holding element to hold the output current value. *Id.* at 28–29 (citing Ex. 1005, 58–59; Ex. 1003 ¶¶ 90–92).

Patent Owner does not dispute these contentions.

We determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests limitation 1f of claim 1 in its teachings relating to the transistor 11 and capacitor 13 acting as a holding element, to hold the output current equal to the offset current of the current amplifier, owing to the electric charge supplied to the capacitor 13 while switch 14 is turned off.

e. Limitation 1g

i. Limitation 1g – Soneda

With respect to limitation 1g, Petitioner argues that Soneda teaches, "the controlled current source, acting as a regulation element in the control loop, is configured to regulate the offset to a minimum by setting a current value of the output current," because Soneda describes that, during a blanking interval, the controlled current source (transistor 11 and capacitor 13) acts as a regulation element by establishing an output current that eliminates the offset current in the output of the entire circuit. Pet. 30–31 (citing Ex. 1005, 58; Ex. 1003 ¶¶ 93–94).

Patent Owner does not dispute Petitioner's contentions with respect to Soneda teaching or suggesting the subject matter of limitation 1g. We determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests the subject matter of limitation 1g.

ii. Limitation 1g – Soneda and Kozisek

Petitioner cites the teachings of Kozisek of a cancellation mode in which voltage at the first terminal will drift until the transistor 62 is biased such that the net current supplied to terminal 68 balances the offset current that will be produced in the amplifier. Pet. 31 (citing Ex. 1006, 6:22–31, Fig. 2; Ex. 1003 ¶¶ 95–96). Petitioner argues that, in light of these teachings, "a POSITA would understand that Soneda's controlled current source—which has a substantially similar configuration to Kozisek's controlled current source acting as a regulation element in the control loop—is configured to regulate the offset to a minimum by setting a current value of the output current." *Id.* at 32 (citing Ex. 1003 ¶ 97). Additionally, Petitioner argues that a combination of Soneda and Kozisek, as discussed with reference to limitation 1e, would have taught or suggested this limitation. *Id.* (citing Ex. 1003 ¶ 98).

With respect to the argument relating to the combination of Soneda and Kozisek, Patent Owner substantially repeats its arguments presented with respect to limitation 1e, which we have addressed above in discussing that claim limitation. Prelim. Resp. 41–42. Patent Owner also presents an argument based on Petitioner's statement that during prosecution of a patent application claiming priority to the '082 patent, Kozisek was cited with respect to this feature, arguing that these facts do not show that one of ordinary skill would have combined Kozisek with Soneda. *Id.* at 42 (discussing Pet. 31). However, Petitioner does not discuss the use of Kozisek by the Examiner of that application in its arguments relating to a motivation to combine, and we do not consider this argument in our

determination with respect to this claim limitation or the Soneda/Kozisek combination. *See* Pet. 31.

On the present record and at this stage of the proceeding, Petitioner has adequately shown that one of ordinary skill in the art would have made the proposed combination. Additionally, Petitioner has shown that in such a combination, the controlled current source regulates the offset to a minimum by setting a current value of the output current, in Kozisek's discussion of a transistor being biased so that net current supplied would balance the output current offset.

Thus, we determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that the combination of Soneda and Kozisek teaches or suggests the subject matter of limitation 1g.

f. Limitation 1h

With respect to limitation 1h, Petitioner argues that Soneda teaches the controlled current source (transistor 11 and capacitor 13) acting to maintain the output from the controlled current source equal to the offset current of the current amplifier, which is supplied during operation intervals. Pet. 32–33 (citing Ex. 1005, 58, 59; Ex. 1003 ¶¶ 99–100).

Patent Owner does not dispute Petitioner's contentions with respect to Soneda teaching or suggesting the subject matter of limitation 1h. We determine that, on this record and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests the subject matter of limitation 1h.

g. Conclusion: Claim 1

We have reviewed the record and determine for the reasons discussed about that, at this stage, Petitioner sufficiently demonstrates a reasonable likelihood of succeeding in its challenges to claim 1.

4. Claims 2–6, 8–11, 13, 14, and 16

Petitioner additionally presents arguments with respects to claims 2–6, 8–11, 13, and 14. Pet. 35–69. Patent Owner presents an argument relating to claim 9, but otherwise does not present additional arguments with respect to these claims.

a. Claims 2–6

Claim 2 depends from claim 1. With respect to the additional recitation of claim 2, Petitioner argues that the recited capacitor is taught in Soneda's capacitor 13. Pet. 37 (citing Ex. 1003 ¶ 108). On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda teaches or suggests the additional subject matter of claim 2.

Claim 3 depends from claim 1. With respect to the additional recitation of claim 3, Petitioner argues that the recitation of the controlled current source being controllable by a control voltage is taught by Soneda's disclosure of the blanking interval, in which the voltage across the capacitor 13 is the gate-source voltage at transistor 11. *Id.* at 37–39 (citing Ex. 1005, 58–59, Fig. 1; Ex. 1003 ¶¶ 109–112). Petitioner alternatively argues that Kozisek teaches this, with reference to the discussion of the voltage at the terminal 66 being charged across the storage capacitor 64. *Id.* at 40–41 (citing Ex. 1006, 6:22–29, 6:38–42; Ex. 1003 ¶¶ 113–115). On the present record, and for the purposes of institution, Petitioner has sufficiently shown

that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claim 3.

Claim 4 depends from claim 1. With respect to the additional recitation of claim 4 and with reference to earlier arguments, Petitioner argues that the claimed "transistor, which by means of a control voltage at a control input, controls the output current of the controlled current source," is taught in Soneda's transistor 11, or alternatively, in the combination of Soneda and Kozisek and in the control input 66 of transistor 62. Pet. 41–42 (citing Ex. 1005, Fig. 1; Ex. 1003 ¶¶ 117–120). On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claim 4.

Claim 5 depends from claim 1, and additionally recites that the controlled current source has a storage device or capacitor for storing a control voltage. Petitioner argues that a capacitor is shown in Soneda's capacitor 13, or in a combination of Soneda and Kozisek, in Kozisek's capacitor 64. Pet. 42–43 (citing Ex. 1006, 6:6–15, 6:22–29, 6:38–42; Ex. 1003 ¶¶ 121–123). On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claim 5.

Claim 6 depends from claim 5, further reciting that the capacitor acts as a regulation element, connectable to the output of the current amplifier by the first switching device. Petitioner refers to its arguments with respect to limitations 1c and 1e. Pet. 44. Additionally, Petitioner argues that the steady state is taught by Soneda's teaching of charging the capacitor until an output signal current is obtained that is unaffected by the offset current. *Id.*

at 44–45 (citing Ex. 1005, 58–59; Ex. 1003 ¶ 126). Alternatively, Petitioner argues that a combination of Kozisek and Soneda would include a steady state attained by capacitor 64, which is charged until "currents in the circuit . . . stabilize." *Id.* at 45 (quoting Ex. 1006, 6:34–37; citing Ex. 1006, 7:25–29; Ex. 1003 ¶¶ 128–129). On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claim 6.

b. Claims 8–10

Claim 8 depends from claim 1, and further recites that the adjusting circuit has a constant current source. Petitioner argues that this is taught or suggested in Kozisek's current source 60 that sources a fixed amount of current. Pet. 46–47 (citing Ex. 1006, 6:1, 6:24–29, Fig. 2; Ex. 1003 ¶¶ 131–132). Petitioner argues that one of ordinary skill would have modified Soneda's adjusting circuit to include Kozisek's constant current source to deal with processing various in the transistors to provide flexibility and would have reasonably expected to succeed in this modification. *Id.* at 47–50 (citing Ex. 1005, 59; Ex. 1006, Fig. 2; Ex. 1003 ¶¶ 133–139). On the present record, and for the purposes of institution, Petitioner has sufficiently shown that a combination of Soneda and Kozisek, teaches or suggests the subject matter of claim 8.

Claim 9 depends from claim 8. Petitioner argues that this claim would have been obvious over a combination of Soneda and Kozisek. Pet. 50–53. Petitioner argues that the current summing node of limitation 9a of claim 9 is taught by second terminal 68 of Kozisek, which is connectable to the output node 46 of the amplifier in Kozisek. *Id.* at 50–51 (citing Ex. 1006, 5:56–68, 6:24–29; Ex. 1003 ¶¶ 140–142).

Patent Owner argues that the current summing node is disclosed in Figure 2a of the '082 patent inside the current amplifier 100. Prelim. Resp. 36. Patent Owner's argument presumes that the language ("current amplifier has a current summing node that is connectable to the output of the current amplifier") of limitation 9a requires the current summing node to be internal to the current amplifier. Prelim. Resp. 36 (annotated version of Fig. 2a); *see id.* at 35–38. Patent Owner argues that, in contrast, the current summing node Petitioner identifies is not part of the current amplifier, but is within the portion of Kozisek Petitioner previously identified as the adjusting circuit of claim 1. *Id.* at 37–38 (citing Pet. 23, 51). We have found Petitioner has shown a likelihood of success with respect to other claims and institute on the basis of those claims. Thus, we will not provide a preliminary determination relating to the construction of limitation 9a (whether the current summing node must be within or "inside" or "part of" a current amplifier) or how the prior art references do or do not teach or suggest the limitation according to the correct construction of this limitation.

With respect to limitations 9b, 9c, and 9d, Petitioner argues that Kozisek teaches a current summing node that sums a first current (the output of transistor 62) and second current (the output of current source 60), as described in those limitations. Pet. 51–53 (citing Ex. 1006, 6:1–15, 6:24–29; Ex. 1003 ¶¶ 143–149). Patent Owner does not present any additional arguments relating to these limitations.

Claim 10 depends from claim 9. With respect to claim 10, Petitioner argues that the additional limitation is taught by Kozisek's disclosure that the output of the transistor 62 enters the summing node with a negative

value, as it "sink[s]" a desired amount of current. *Id.* at 53–54 (citing Ex. 1006, 6:14–15; 1003 ¶¶ 150–151).

c. Claims 11, 13, 14, and 16

Claim 11 depends from claim 1, and adds the limitation that the adjusting circuit have a second switching device that is connectable via an input of the adjusting circuit to the output of the current amplifier and the circuit output. Petitioner argues that this is shown in Soneda's switch 6, which connects the input of the adjusting circuit to the output of the current amplifier and the output of the circuit. Pet. 55–56 (citing Ex. 1005, 58, Fig. 1; Ex. 1003 ¶¶ 153–154).

Claims 13 and 14 depend from claims 1 and 11 respectively, each adding a limitation relating to control circuitry to control a switching device. Petitioner argues, with respect to each claim, that one of ordinary skill in the art would have understood Soneda's circuit to include a control circuit to control the timing to turn on and turn off the switches, and that this control circuit would be connectable to a control terminal of the switch. *Id.* at 57, 60–61 (citing Ex. 1005, 59; Ex. 1003 ¶¶ 156, 161).

With respect to each claim, Petitioner additionally argues that Kozisek describes a control circuit for selecting the modes of the differential amplifier. *Id.* at 57–58, 61 (citing Ex. 1006, 3:19–37, 7:60–8:37, Fig. 5 (elements 110, 112); Ex. 1003 ¶¶ 157, 162)). Petitioner argues that one of ordinary skill would have used Kozisek's control circuitry in Soneda's circuit to control the precise timing and allow ease of adjustment, and that one of ordinary skill in the art would have reasonably expected to succeed in this modification. *Id.* at 58–61 (citing Ex. 1008, 4:7–11, 4:19–35; Ex. 1003 ¶¶ 158–159, 162)).

Claim 16 depends from claim 1, and further requires the circuit to comprise a control circuit configured to perform certain steps of connection and disconnection by opening and closing the first switching device and opening and closing a second switching device. Petitioner references its arguments with respect to claims 13 and 14 for the showing of the control circuit. Pet. 62. Petitioner contends Soneda teaches these steps and the disconnections and connections with reference to switch 6 of Soneda (corresponding in Petitioner's argument to the second switching device) and switch 14 of Soneda (corresponding in Petitioner's argument to the first switching device) and Soneda's blanking and operation intervals. *Id.* at 62–69 (citing Ex. 1005, 58–59, Figs. 1, 2; Ex. 1003 ¶¶ 166–-177).

Patent Owner does not present additional arguments with respect to the additional limitations of claims 11, 13, 14, and 16.

On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claims 11, 13, 14, and 16.

5. Claim 17

Petitioner argues that claim 17 would have been obvious over Soneda or over a combination of Soneda and Kozisek. Pet. 34–37. Petitioner argues that Soneda teaches a method for correcting an offset of an output current of a current amplifier of a circuit. *Id.* at 34 (citing Ex. 1005, 57, 58; Ex. 1003 ¶ 102). Petitioner argues limitations 17a and 17c of claim 17 with reference to its contentions with respect to limitations 1e, 1f, and 1h of claim 1, which we have discussed above, along with Patent Owner's arguments regarding limitation 1e, in Section IV.D.3.

With respect to limitation 17b, Petitioner refers to its arguments with respect to limitation 1g, which we have already discussed, and additionally argues that Soneda teaches setting a current value of the output current of the controlled current source (as discussed with respect to limitation 1g) when the input signal of the current amplifier has a constant value, because during the blanking interval of Soneda, the input signal of the current amplifier is zero, as switch 2 is described as being turned off. *Id.* at 35–36 (citing Ex. 1005, 59, Fig. 1; Ex. 1003 ¶ 106).

Patent Owner contends that Soneda does not show that the input signal of the current amplifier has a constant value, because "Petitioner never identifies anywhere that Soneda teaches holding an input signal at a constant value" but rather "arbitrarily selects the point immediately after a switch in the middle of the purported current amplifier of Soneda as the input without addressing the express teachings of Soneda." Prelim. Resp. 21, 30–31. Patent Owner argues that Petitioner has identified the current amplifier as including switch 2, and that this is inconsistent because "Petitioner then argues that the input to its purported current amplifier is an arbitrary point in the middle of the current amplifier." *Id.* at 31–33 (reproducing and discussing Petitioner's annotated figure 1 of Soneda from Pet. 14 and comparing it to the annotated figure 1 of Soneda from Pet. 36). However, immediately prior to this annotated figure 1, Petitioner identifies and discusses Soneda's disclosure of a current amplifier as shown in Soneda's Figure 5, which does not include a switch such as switch 2. Pet. 13. On the present record, Petitioner has not selected "an arbitrary point in the middle of the amplifier" as the input, and has shown that the input signal would be constant if switch 2 were turned off, as Soneda teaches during its

blanking interval, but rather has presented an input consistent with its arguments relating to the current amplifier, if not to one of its explanatory annotated figures.

On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claim 17.

6. Claims 18–22, 24–27, and 29–32

Petitioner argues claims 18–22, 24–27, and 29–31 on the same basis as that previously discussed with respect to claims 2–6, 8–11, and 13–15, respectively. Pet. 37–69. Patent Owner presents no additional arguments with respect to these claims.

Therefore, on the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claims 18–22, 27, and 29–31 and that Soneda in combination with Kozisek teaches or suggests claim 24. With respect to claims 25 and 26, these claims are subject to the same issues we discuss above with respect to claims 9 and 10. *See supra* § IV.D.4.b.

E. Claims 7 and 23

Petitioner argues that claims 7 and 23 would have been obvious over a combination of Soneda, Kozisek, and Palmisano. Pet. 71–75. Claim 7 depends from claim 1, adding the limitation that "the current amplifier has a first current mirror and a second current mirror for current amplification, whose outputs are connected to the output of the current amplifier," and claim 23 depends from claim 17, adding the same additional limitation. Ex. 1001, 10:54–57, 12:9–12.

Petitioner argues that Palmisano describes a mirrored current amplifier with a first and second mirror, and that the outputs are connected to the output of the current amplifier. Pet. 71–72 (citing Ex. 1007, 47, Fig. 2.2; Ex. 1003 ¶¶ 184–187). Petitioner additionally argues that one of ordinary skill would have modified Soneda's circuit to include a current amplifier with two mirrors as in Palmisano to include a well-known design for an amplifier, improving the performance at lower voltage, simplifying the design, and reducing distortion and noise, and would have reasonably expected to be successful in doing so. *Id.* at 73–75 (citing Ex. 1003 ¶¶ 188–189).

Patent Owner presents no additional arguments with respect to these claims.

On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claims 7 and 23.

F. Claims 12, 15, 28, and 31

Petitioner argues that claims 12, 15, 28, and 31 would have been obvious over a combination of Soneda, Kozisek, and Gutzki. Pet. 61, 75–81.

Claim 12 is dependent from claim 1 and adds the requirement that the adjusting circuit of claim 1 "has a second switching device, which is connectable to a capacitor and is configured to discharge the capacitor in a closed state." Ex. 1001, 11:11–14. Claim 28 is dependent from claim 17, and adds the requirement that "an adjusting circuit has a second switching device, which is connectable to a capacitor and is configured to discharge the capacitor in a closed state." *Id.* at 12:32–35.

Petitioner argues that Gutzki teaches these claim limitations in its description of an offset compensation circuit that includes a capacitive storage element (element 22 of Gutzki's Figure 1) and switches that provide a discharge circuit for the storage element 22 that completely discharges that storage element. Pet. 78 (citing Ex. 1008, 3:57–64, 4:44–67; Ex. 1003 ¶¶ 190–191). Petitioner further argues that one of ordinary skill would have been motivated to combine this teaching of Gutzki and Soneda's adjusting circuit to ensure that the initial voltage of the capacitor is in a known state and eliminates a possibility of a high initial voltage that might impair operations, and would have reasonably expected to succeed in this modification. *Id.* at 79–81 (citing Ex. 1003 ¶¶ 193–194).

Petitioner argues claims 15 and 31 on the basis of its arguments with respect to claims 12 and 28 and with respect to the arguments regarding claim 14. Pet. 61.

Patent Owner presents no additional arguments with respect to these claims.

On the present record, and for the purposes of institution, Petitioner has sufficiently shown that Soneda, alone or in combination with Kozisek, teaches or suggests the subject matter of claims 12, 15, 28, and 31.

V. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition. We decline also to exercise our discretion to deny institution under 35 U.S.C. § 314(a).

VI. ORDER

Accordingly, it is:

ORDERED that *inter partes* review of claims 1–32 of the ’082 patent is instituted on all grounds in the Petition;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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