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Paper 19
Entered: January 30, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

TELA INNOVATIONS, INC.,
Patent Owner.

IPR2019-01228
Patent 7,943,966 B2

Before JO-ANNE M. KOKOSKI, KRISTINA M. KALAN, and WESLEY B. DERRICK, *Administrative Patent Judges.*

KALAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 2, 31–33, and 35 of U.S. Patent No. 7,943,966 B2 (Ex. 1001, "the '966 patent"). Petitioner concurrently filed two other petitions for *inter partes* review of the challenged claims, in IPR2019-01220 ("the 1220 IPR") and IPR2019-01221 ("the 1221 IPR"). *Intel Corp. v. Tela Innovations, Inc.*, IPR2019-01220, Paper 2 (PTAB June 20, 2019); *Intel Corp. v. Tela Innovations, Inc.*, IPR2019-01221, Paper 2 (PTAB June 20, 2019).

Tela Innovations, Inc. ("Patent Owner") filed a Preliminary Response to the Petition (Paper 11, "Prelim. Resp."). Patent Owner does not substantively address the merits of Petitioner's challenge, but contends review by the Board would be improper. *See generally* Prelim. Resp. We authorized additional briefing on the issues set forth in the Preliminary Response. Paper 14. Petitioner in turn filed a Reply to Patent Owner's Response (Paper 16, "Reply") and Patent Owner filed a Sur-Reply to Petitioner's Reply (Paper 18, "Sur-Reply").

Additionally, as authorized by our Order (Paper 13, "Notice Order"), Petitioner filed a Notice Ranking Petitions (Paper 15, "Notice"), and Patent Owner filed a Response (Paper 17). In the Notice, Petitioner requested that we consider the current Petition before the 1220 IPR petition, and sought to withdraw the 1221 IPR petition. Notice 2. In an Order (1221 IPR, Paper 19), we allowed Petitioner to file a motion to dismiss the 1221 IPR petition. Petitioner filed a Motion to Dismiss the 1221 IPR petition (1221 IPR, Paper 20), and we dismissed the 1221 IPR petition (1221 IPR, Paper 21).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a). To institute an *inter partes*

review, we must determine that the information presented in the Petition shows that there is "a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Applying that standard, for the reasons set forth below, we institute an *inter partes* review as to all challenged claims and the ground raised in the Petition.

A. Related Proceedings

The parties identify a civil action involving Petitioner in the Northern District of California, *Intel Corp. v. Tela Innovations, Inc.*, Case No. 3:18-cv-02848-WHO (N.D. Cal.), filed May 15, 2018 ("the NDCA Action"). Pet. 2; Paper 4, 2. This action was filed as a declaratory judgment action involving a number of Patent Owner's patents, including the '966 patent. Pet. 3; Paper 4, 2. The parties identify further civil actions, to which Petitioner is not a party, involving the '966 patent. Pet. 3; Paper 4, 2.

The parties also identify an International Trade Commission ("ITC") proceeding, Inv. No. 337-TA-1148, In the Matter of Certain Integrated Circuits and Products Containing the Same, filed December 19, 2018 ("the ITC Proceeding"), as a proceeding involving the '966 patent that was pending when the Petition was filed. Pet. 2; Paper 4, 1; Prelim. Resp. 13–15. Patent Owner explains that the '966 patent has been terminated from the ITC Proceeding. Prelim. Resp. 15.

The parties identify the two additional petitions that Petitioner filed requesting an *inter partes* review of the same claims of the '966 patent challenged in this proceeding, namely, the 1220 IPR and the 1221 IPR. Pet. 3; Paper 4, 2.

B. The ’966 Patent

The ’966 patent, titled “Integrated Circuit and Associated Layout With Gate Electrode Level Portion Including at Least Two Complimentary Transistor Forming Linear Conductive Segments and at Least One Non-Gate Linear Conductive Segment,” is directed to a layout of a semiconductor device. Ex. 1001, code (54), 7:63–64. The ’966 patent explains that a push for circuit chip area reduction in the semiconductor industry has resulted in improvements in the lithographic process that enable smaller feature sizes to be achieved. *Id.* at 7:19–31. In the evolution of lithography, the minimum feature size approached, and subsequently passed, the wavelength of the light source to expose the feature shapes, and unintended actions occurred between neighboring features. *Id.* at 7:32–35. The ’966 patent describes the difference between the minimum feature size and the wavelength of light used in the photolithography process as the lithographic gap. *Id.* at 7:38–40. The ’966 patent further describes that an interference pattern occurs as each shape on the mask interacts with the light. *Id.* at 7:43–44. The interference patterns from neighboring shapes can create constructive or destructive interference. *Id.* at 7:44–46. In view of the foregoing, the ’966 patent identifies a need for a solution that manages lithographic gap issues as technology progresses toward smaller semiconductor device feature sizes. *Id.* at 7:57–59.

The ’966 patent describes that a dynamic array architecture is provided to address semiconductor manufacturing process variability associated with a continually increasing lithographic gap. *Id.* at 10:6–9. Figure 2 of the ’966 patent, shown below, illustrates a generalized stack of layers used to define a dynamic array architecture.

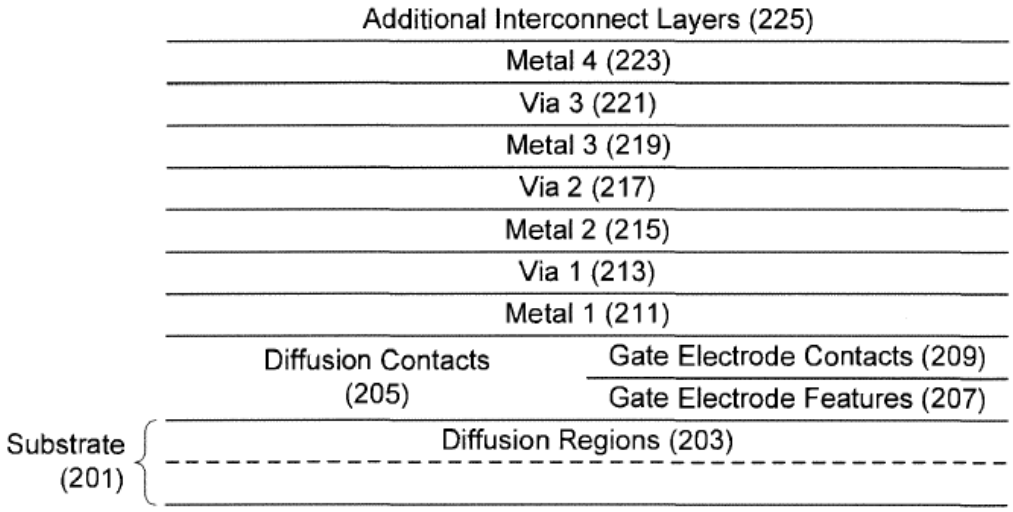

Fig. 2

Figure 2 depicts the generally underlying structure of a dynamic array. *Id.* at 12:10–26. The dynamic array is built up in a layered manner upon base substrate 201 (*e.g.*, a silicon substrate or silicon-on-insulator (SOI) substrate). *Id.* at 12:26–28. Diffusion regions 203 are defined in base substrate 201, where diffusion regions 203 represent selected regions of base substrate 201 within which impurities are introduced for the purpose of modifying the electrical properties of base substrate 201. *Id.* at 12:28–33. Above diffusion regions 203, diffusion contacts 205 are defined to enable connection between diffusion regions 203 and conductor lines. *Id.* at 12:33–35. Gate electrode features 207 are defined above diffusion regions 203 to form transistor gates. *Id.* at 12:38–40. Gate electrode contacts 209 are defined to enable connection between gate electrode features 207 and conductor lines. *Id.* at 12:40–42. Interconnect layers are defined above diffusion contact 205 layer and gate electrode contact layer 209. *Id.* at 12:45–46. Interconnect layers include first metal layer 211 (metal 1), first via layer 213 (via 1), second metal layer 215 (metal 2), second via layer 217

(via 2), third metal layer 219 (metal 3), third via layer 221 (via 3), and fourth metal layer 223 (metal 4). *Id.* at 12:46–51.

Figure 5 of the ’966 patent, shown below, illustrates an example layout of a dynamic array.

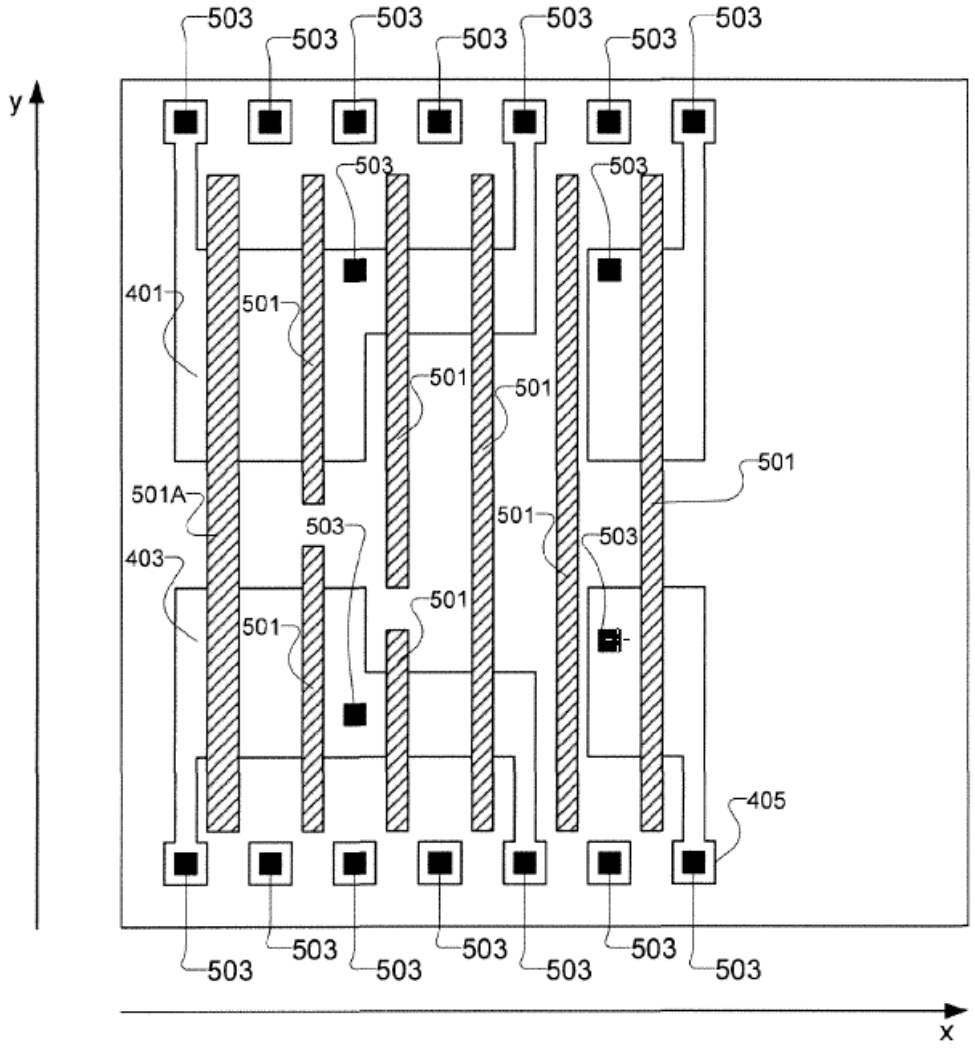

Fig. 5

Figure 5 depicts an example layout of a dynamic array including a gate electrode layer, a diffusion contact layer, and a diffusion layer. *Id.* at 17:6–9. The gate electrode layer shows gate electrode features 501 that define the transistor gates. *Id.* at 17:9–11. Gate electrode features 501 are defined as

linear shaped features extending in a parallel relationship across the dynamic array in a "y" reference direction. *Id.* at 17:11–13. Gate electrode features 501 form n-channel and p-channel transistors as they cross diffusion regions 403 and 401, respectively. *Id.* at 17:27–29. The '966 patent describes that each of the gate electrode tracks may be interrupted any number of times in linearly traversing across the dynamic array in order to provide required electrical connectivity for a particular logic function to be implemented. *Id.* at 17:38–41. When a given gate electrode track is required to be interrupted, the separation between ends of the gate electrode track segments at the point of interruption is minimized to the extent possible. *Id.* at 17:41–46. Minimizing the separation between ends of the gate electrode track segments at the points of interruption serves to maximize the lithographic reinforcement, and uniformity therefor, provided from neighboring gate electrode tracks. *Id.* at 17:49–52.

Figure 8B of the '966 patent, shown below, illustrates another example layout of a dynamic array.

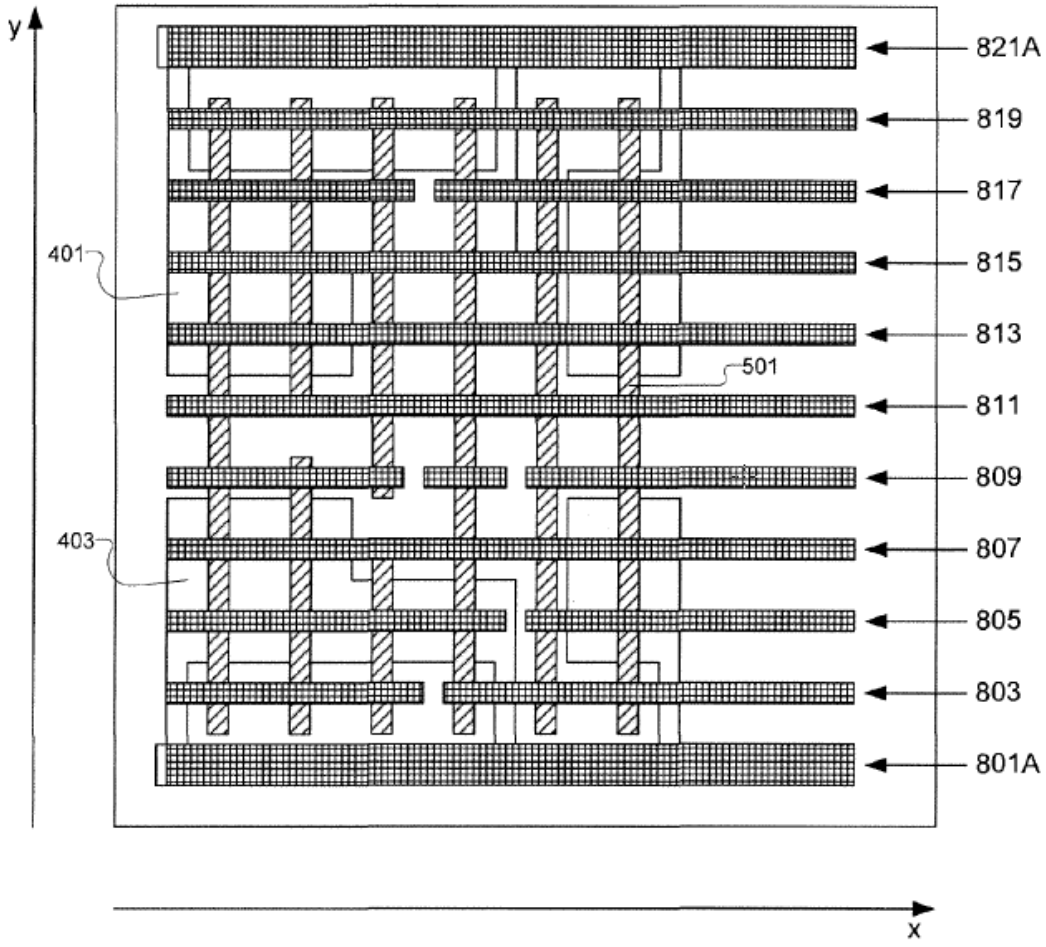

Fig. 8B

Figure 8B depicts metal 1 layer defined above the gate electrode layer of Figure 5, in accordance with one embodiment of the invention. *Id.* at 19:67–20:3. Metal 1 layer includes a number of metal 1 tracks 803–819 and power tracks 801A and 821A. *Id.* The metal 1 tracks include linear-shaped features extending in a parallel relationship across the dynamic array. *Id.* at 19:23–26.

C. Illustrative Claim

2. An integrated circuit device, comprising:
a substrate region that forms part of an overall substrate of the integrated circuit device,

a gate electrode level region that forms part of an overall gate electrode level of the integrated circuit device, the gate electrode level region formed above and over the substrate region, wherein the gate electrode level region includes a plurality of linear conductive segments each formed to have a respective length and a respective width as measured parallel to the substrate region, wherein a size of the length of a given linear conductive segment is greater than or equal to a size of the width of the given linear conductive segment, wherein the plurality of linear conductive segments are formed to have their lengths extend in a first direction in a parallel manner, and

wherein the plurality of linear conductive segments are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction, and

wherein the plurality of linear conductive segments include a first linear conductive segment defined to form both a gate electrode of a first transistor of a first transistor type and a gate electrode of a first transistor of a second transistor type, and

wherein the plurality of linear conductive segments include a second linear conductive segment that does not form a gate electrode of a transistor device, and

wherein the plurality of linear conductive segments include a third linear conductive segment defined to form both a gate electrode of a second transistor of the first transistor type and a gate electrode of a second transistor of the second transistor type.

Ex. 1001, 27:39–28:5.

D. The Asserted Ground of Unpatentability

Petitioner contends claims 2, 31–33, and 35 of the ’966 patent are unpatentable on the following ground:

Reference	Basis	Claims Challenged
Ichiryu[1]	§ 103	2, 31, 32, 33, 35

In support of its unpatentability arguments, Petitioner relies on the declaration testimony of Dr. Stanley Shanfield. Ex. 1002.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art "would have been a person having a Bachelor's degree in Electrical Engineering, Physics or Materials Science with three to five years of industry experience in semiconductor integrated circuit design, layout or fabrication," but that "[a]dditional education might compensate for a deficiency in experience, and vice-versa." Pet. 18 (citing Ex. 1002 ¶¶ 61–64). Patent Owner neither disputes Petitioner's articulation of the level of ordinary skill in the art nor presents its own articulation of the level of skill in the art.

On this record, we have no reason to fault Petitioner's definition of the level of ordinary skill and, therefore, adopt it for the purposes of this Decision. We further note that the prior art itself demonstrates the level of skill in the art at the time of the invention. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that "specific findings on the level of skill in the art . . . [are not required] 'where the prior art itself reflects an appropriate level and a need for testimony is not shown'" (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))).

[1] US 7,503,026 B2, issued Mar. 10, 2009 (Ex. 1013).

B. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b); *see also Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (applicable to *inter partes* reviews filed on or after November 13, 2018). Under *Phillips*, claim terms are afforded "their ordinary and customary meaning." *Phillips*, 415 F.3d at 1312. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner does not believe the claim terms of the '966 patent require express construction for the purposes of evaluating the prior art in the Petition. Pet. 20. However, Petitioner provides constructions of the claim terms "linear," "gate electrode," and "interconnect level region" that it proposed in the NDCA Action, and contrasts them to the constructions that Patent Owner proposed in that district court action. Pet. 18–25. Patent Owner does not propose any constructions for any claim terms of the '966 patent. *See generally* Prelim. Resp. We decline to construe any claim term of the '966 patent, because it is not necessary to do so in reaching our decision that Petitioner has established a reasonable likelihood that it would prevail in establishing the unpatentability of at least one challenged claim.

C. Principles of Law

A claim is unpatentable under § 103 if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) as "requiring *inter partes* review petitions to identify 'with particularity . . . the evidence that supports the grounds for the challenge to each claim'"); *cf. Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (quoting 35 U.S.C. § 312(a)(3)) (addressing "the requirement that the initial petition identify 'with particularity' the evidence that supports the grounds for the challenge to each claim'"). This burden never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (citing *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1326–27 (Fed. Cir. 2008)) (discussing the burden of proof in *inter partes* review). Furthermore, Petitioner cannot satisfy its burden of proving

obviousness by employing "mere conclusory statements." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Thus, to prevail in an *inter partes* review grounded on alleged obviousness, Petitioner must explain how the proposed combinations and/or alterations of the prior art would render the challenged claims unpatentable as obvious. At this stage, we determine whether the information in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been obvious over the proposed combinations and/or alterations of the prior art.

D. Patent Owner's Arguments

Patent Owner contends that Petitioner has engaged in a duplicative litigation strategy that warrants denial of institution of this *inter partes* review. *See generally* Prelim. Resp. Patent Owner highlights, as duplicative, the NDCA Action, the ITC Proceeding, and the additional petitions filed seeking *inter partes* review of the '966 patent, as well as petitions filed seeking *inter partes* review of other, related patents. Patent Owner contends that: (i) the Petition is statutorily barred under 35 U.S.C. § 315(a)(1) because Petitioner initiated a challenge to the validity of the '966 patent prior to filing the Petition; and (ii) the Board should deny institution under 35 U.S.C. § 314(a) because of overlap between this Petition, the NDCA Action, the ITC Proceeding, and the multiplicity of petitions seeking an *inter partes* review of this, and related, patents. We address each of these arguments in turn below.

1. 35 U.S.C. § 315(a)(1)

Section 315 sets forth that " inter partes review may not be instituted if, before the date on which the petition for such a review is filed, the

petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent." 35 U.S.C. § 315(a).

Patent Owner contends that Petitioner's Declaratory Judgment Complaint in the NDCA Action (the "DJ Complaint") triggers the statutory bar despite not expressly pleading invalidity as a cause of action. *See generally* Prelim. Resp. 29–34. Petitioner disagrees that anything less than an express pleading of the cause of action of invalidity suffices, and contests Patent Owner's contentions supporting its case. *See generally* Reply 2–7. On this record, as discussed below, we do not find that Petitioner's DJ Complaint seeks a declaration that any claim of the '966 patent is invalid, or that the DJ Complaint triggers the statutory bar.

Patent Owner contends that, although "Intel couched its claims in the Complaint in the NDCA Action as a declaratory judgment action for non-infringement, that pleading also included detailed allegations that Tela's attempts to apply the Patents-in-Suit to Intel's products would render Tela's patents invalid because Intel's technology was developed by Intel first." Prelim. Resp. 30 (citing Ex. 2002 ¶¶ 22–38, 44); *see also id.* at 6–8 (citing Ex. 2002 ¶¶ 22–29, 44, 49–52). Patent Owner also notes that these allegations are repeated in the first and second amended complaints. *Id.* (citing Ex. 2003 ¶¶ 22–38, 44; Ex. 2007 ¶¶ 27–44, 50). Patent Owner highlights, in particular, the conclusion in the complaints:

> [B]ecause Intel's technology used in its commercial products since at least 2007 [. . .] was developed by Intel well before any of Tela's patents were conceived, and before Tela was even created, Intel's products cannot be covered by Tela's patents. And Tela's attempts to apply those patents to Intel's products **would render Tela's patents invalid** because Intel's technology was developed by Intel first.

Id. at 30–31 (citing Ex. 2002 ¶ 44; Ex. 2003 ¶ 44, Ex. 2007 ¶ 50); *see also* Sur-Reply 3 (citing Ex. 2002 ¶ 44; Ex. 2003 ¶ 44; Ex. 2007 ¶ 50). Patent Owner argues that these allegations "are a direct challenge to the validity of the '966 Patent and should invoke the statutory bar under Section 315(a)(1)." Prelim. Resp. 31. Patent Owner further argues that these allegations "were expressly incorporated into Intel's causes of action." Sur-Reply 3–4 (citing Ex. 2002 ¶ 49; Ex. 2003 ¶ 50; Ex. 2007 ¶ 77).

Patent Owner contends that Petitioner's allegations in the DJ Complaint suffice to constitute a validity challenge within the meaning of Section 315(a)(1), because the allegations go beyond "general statements that a party does not infringe any 'valid claim,'" which the Board has found insufficient to trigger the Section 315(a)(1) in other proceedings, because Petitioner "provided substantive and detailed factual allegations to support an express assertion of invalidity of the '966 Patent." Prelim. Resp. 31 (citing *LG Elecs., Inc. v. Straight Path IP Grp., Inc.*, IPR2015-00196, Paper 56 at 16–17 (PTAB May 9, 2016); Ex. 2002 ¶¶ 22–38, 44; Ex. 2003 ¶¶ 22–38, 44; Ex. 2007 ¶¶ 27–44, 50).

Petitioner responds that the DJ Complaint is devoid of a cause of action for invalidity and, thus, does not trigger the statutory bar. Reply 3–6. Petitioner highlights that Patent Owner admits this by stating that "Intel couched its claims in the complaint in the NDCA Action as a declaratory judgment action for ***non-infringement***," and Petitioner argues that the Complaint's recitation that "Intel's products 'do not infringe . . . any valid and enforceable claim' of the '966 Patent" "does not turn a case of action of non-infringement into a validity challenge that would trigger a statutory bar." *Id.* at 3 (quoting Prelim Resp. 8; Ex. 2002 ¶¶ 51–52). Petitioner further highlights that the Board focuses on "the cause of action" when

assessing whether a complaint triggers a statutory bar, and Petitioner argues that the "Background Section" of the DJ Complaint that Patent Owner relies on to explain "how 'Intel Invented the Technology of the Patents-In-Suit Before Tela'" "does not constitute a cause of action." *Id.* at 4 (quoting Prelim. Resp. 6–8 (citing Ex. 2002 ¶¶ 22–38, 44)).

We disagree with Patent Owner's arguments that the DJ Complaint expressly alleges invalidity. Although the DJ Complaint includes assertions of earlier technology development, this is not the same as alleging invalidity of patent claims. Ex. 2002 ¶¶ 22–38. Similarly, we do not find Petitioner's contention as to the proper claim scope to constitute an allegation of invalidity of patent claims, even if it indicates that an improper scope would render patents invalid. *Id.* ¶ 44. The import of the DJ Complaint can be understood by the fact that it includes, for example, that Patent Owner, in an earlier ITC action against several handset manufacturers, had contended its "patents required strictly one-dimensional conductive structures in the gate layer and were different from [Petitioner's] gridded layout technology with two-dimensional conductive structures." *Id.* ¶¶ 30, 37. The DJ Complaint incorporates this, and the section detailing the earlier technology development, into its counts seeking declaratory judgment of non-infringement and causes of action other than invalidity. *See, e.g.*, *id.* ¶¶ 53–56, 124–144. This is consistent with Petitioner's contention that the DJ Complaint is devoid of a cause of action for invalidity of the '966 patent.

Patent Owner also contends: "The fact that Intel's claims are captioned as being related to non-infringement and other theories does not prevent application of Section 315(a)(1)." Prelim. Resp. 32; *see also* Sur-Reply 4 (contending that "Section 315(a)(1) nowhere states that it is limited to causes of action labelled as 'invalidity' claims"). Patent Owner relies on

three Federal Circuit decisions to support this contention. Prelim. Resp. 32–33.

First, Patent Owner relies on *Totes-Isotoner Corp. v. United States* to support its contention that, "[w]ith respect to pleadings, it is understood that a court looks 'to the quality of its substance rather than according to its form or label.'" Prelim. Resp. 32 (quoting *Totes-Isotoner Corp. v. United States*, 594 F.3d 1346, 1358 (Fed. Cir. 2010) (internal citation omitted)); *see also* Sur-Reply 4. In *Totes-Isotoner*, the issue was whether the pleading included "'a short and plain statement of the claim showing that the pleader is entitled to relief,' in order to 'give the defendant fair notice of what the . . . claim is and the grounds upon which it rests.'" *Totes-Isotoner*, 594 F.3d at 1354 (quoting *Bell Atl. Corp. v. Twombly*, 550 U.S. 544, 555 (2007) (quoting *Conley v. Gibson*, 555 U.S. 41, 47 (1957))). The distinction as to the pleadings' form or label was whether provisions of tariff classification were facially discriminatory or discriminatory on the basis they caused disparate impact. *Id.* at 1358 n.6. Both labels for the pleadings in *Totes-Isotoner* related to discrimination as the cause of action, as did the underlying substance, differing from this case in that what is nominally pled and what Patent Owner contends is pled are wholly different causes of action, e.g., non-infringement and invalidity. Patent Owner fails to address this difference, or sufficiently explain how what is made out is a sufficient pleading for declaratory judgment of invalidity.

Second, Patent Owner relies on *Air Products & Chemicals, Inc. v. Reichhold Chemicals, Inc.* to support the contentions that "[t]he fact that a cause of action has been couched in terms of patent infringement is not dispositive as to whether the case arises under the patent laws" and that "in determining subject matter jurisdiction, the court must consider as a whole

the substance of the claim in addition to the language of the complaint, and may also consider jurisdictional facts outside the pleadings." Prelim. Resp. 32 (quoting *Air Prods. & Chems., Inc. v. Reichhold Chems., Inc.*, 755 F.2d 1559, 1561 (Fed. Cir. 1985)). In *Air Products*, the issue was whether the cause of action arose under the patent laws, not what declaratory relief was sought. *Air Prods.*, 755 F.2d at 1561. Accordingly, *Air Products* is not support for the DJ Complaint setting forth a different cause of action than that explicitly pled.

Third, Patent Owner relies on *Brazos Electric Power Cooperative, Inc. v. United States* to support its contention "that artful pleading should not be permitted to avoid statutory implications." Prelim. Resp. 32 (citing *Brazos Elec. Power Coop., Inc. v. United States*, 144 F.3d 784, 787 (Fed. Cir. 1998)). In *Brazos Electric*, the court found cancellation of debt just as much a form of monetary damages as direct payment of conventional monetary damages for purposes of determining jurisdiction. *Brazos Elec.*, 144 F.3d at 787. No such equivalence is apparent, however, in the declaratory relief sought in the DJ Complaint and a declaratory judgment of invalidity.

Patent Owner further relies on Board decisions Petitioner cites in the Reply, contending that these support Patent Owner's position rather than Petitioner's. Sur-Reply 3–6. For example, Patent Owner argues that the Board's holding "that a complaint that 'only alleges a cause of action of noninfringement,' not invalidity, is 'not considered a filing of a civil action for invalidity under 35 U.S.C. § 315(a)(1),'" supports its position that the statutory bar applies because here, "the Complaints expressly alleged invalidity." Sur-Reply 5 (quoting *Samsung Elecs. Co., Ltd. v. Bitmicro, LLC*, IPR2018-01410, Paper 14 at 20 (PTAB Jan. 23, 2019)). Patent Owner

similarly argues that a Board decision that "confirms Congress intended 'a civil action challenging the validity of a claim of a patent' to be limited to a declaratory judgment action for invalidity, not an antitrust action" supports its position that the statutory bar applies because Petitioner "sought a declaratory judgment based on claims that directly and expressly incorporated assertions of invalidity." *Id.* at 6 (citing *Am. Nat'l. Mfg., Inc. v. Sleep No. Corp.*, IPR2019-00514, Paper 10 at 11 (PTAB Aug. 5, 2019)).

We disagree with Patent Owner. As an initial matter, we are not persuaded on this record that the DJ Complaint expressly alleges invalidity, as Patent Owner argues. In addition, Patent Owner does not direct us to any authority demonstrating that the Board has interpreted 35 U.S.C. § 315(a)(1) in the manner it proposes. In particular, even if Petitioner's causes of action in the DJ Complaint did "incorporate assertions of invalidity" by reference, as Patent Owner contends, the complaint still does not allege a cause of action for invalidity. Rather, at best, the DJ Complaint sets forth causes of action grounded on factual assertions that might support a different cause of action (a declaration that claims are invalid). That, however, does not distinguish this case from *Samsung Electronics* (where the declaratory judgment complaint did not allege a cause of action for invalidity), or *American National Manufacturing* (where the declaratory complaint alleged an antitrust violation and did not challenge the patent's validity). Thus, Patent Owner directs us to no authority excusing this requirement for triggering a bar under 35 U.S.C. § 315(a)(1).

Patent Owner further contends that the district court's perception of Petitioner's allegations and Petitioner's counsel's statements in the NDCA Action support Patent Owner's contention that the action seeks declaratory relief for invalidity. Prelim. Resp. 9–10, 30–31; Ex. 2004, 1; Ex. 2005, 9–

10. Patent Owner relies on the court's statement that "Intel now brings this action seeking declaratory relief for noninfringement, invalidity, and unenforceability with respect to six Tela patents" in an order, dated September 18, 2018, addressing a motion to transfer venue and motions to seal. Prelim. Resp. 9, 31; Ex. 2004, 1. Patent Owner also refers to statements made by Petitioner's counsel during an October 3, 2018, hearing "that the prior art materials relied upon should not be produced until the time required for invalidity contentions," and argues that these statements "confirm that Intel was directly and expressly challenging validity." Prelim. Resp. 31–32 (citing Ex. 2005, 9–10). Patent Owner contends that, during the hearing, it "disputed Intel's production of materials related to the prior art relied on by Intel to support its allegations of invalidity in paragraph 44 of . . . the Complaint" and that "[d]uring that hearing, [it] requested production of the prior art relied on for those invalidity allegations." *Id.* at 9 (citing Ex. 2005, 9–10). Patent Owner further contends that, "[i]n response, Intel's counsel argued that its invalidity contentions regarding its asserted prior art should not be produced until after Tela provided infringement contentions in accordance with the NDCA Patent Local Rules," stating:

> So really what the issue is here is they want to turn the local rules on their head and they want the contentions on validity first so they can pick their claims. That's something that every patentee could say in every single patent case: We want to see what you have first. the local rules set out the procedure. You pick the products, then we come up with the prior art. And we see no reason to deviate from the normal local rules. This is just a piece of prior art.

Prelim. Resp. 9–10 (citing Ex. 2005, 9–10); *see* Sur-Reply 2. Patent Owner contends that these are Petitioner's admissions that are "direct evidence that

Intel was pursuing an invalidity challenge under the guise of non-infringement claims." Sur-Reply 2 (citing Ex. 2004, 1).

Petitioner contests Patent Owner's reliance on the court's statement in the order, and argues that the statement from the hearing is taken out of context to support Patent Owner's assertion that the DJ Complaint challenged validity. Reply 6 (citing Prelim. Resp. 9–10). Petitioner highlights that "Patent Owner's lead counsel . . . sought to correct the Court's misperception that Petitioner's DJ complaint challenged validity of its patents, and confirmed Patent Owner's understanding that it did not:

> [I]n Your Honor's prior order you had indicated -- I think you believed that Intel had alleged invalidity of patents. ***They've gone out of their way not to allege invalidity of the patents***.

Id. (citing Ex. 2005, 6:15–22 (with added emphasis)).

On this record, we discern no sound basis for Patent Owner's reliance on the statements made in the order and hearing in the NDCA Action as support for its positions. As Petitioner highlights, counsel for Patent Owner expressly set forth that Petitioner had "gone out of their way not to allege invalidity of the patents," apparently correcting the court's characterization of the DJ Complaint. Ex. 2005, 6:15–22. We also find that Patent Owner's contention that Petitioner's counsel's statements are evidence that Petitioner was pursuing an invalidity challenge lacks support on this record. Preceding the statement from Petitioner's counsel (Mr. Arovas) that Patent Owner cites, counsel for Patent Owner (Mr. Belanger) states that Petitioner "allege[s] that if we were to assert infringement . . . we would be committing patent misuse because we would be accusing something that they claim was in the prior art." *Id.* at 8:23–9:1. And immediately following the statement

from Petitioner's counsel on which Patent Owner relies, counsel for Patent Owner responds that:

> we would respectfully disagree, particularly given the discussion we just had, Your Honor, about the declaratory judgment standing here. What Intel has alleged is not merely a garden variety invalidity case based on public information. That's absolutely not what they're alleging . . . [w]hat they're alleging is that they had secret internal documents, . . . that form the basis of a patent misuse claim if we were to assert infringement . . . . They're the ones who made the claim of patent misuse based on information that's not known to our client.

Id. at 10:3–18. Patent Owner fails to explain how what the parties are discussing is anything other than a patent misuse claim, or how such a claim constitutes a civil action for invalidity. *See generally* Prelim. Resp.; Sur-Reply.

Patent Owner also contends that Petitioner's allegations in the DJ Complaint and amended complaints filed in the NDCA Action "essentially amount to a practicing the prior art argument" and that this "triggers the Section 315(a)(1) bar to institution." Prelim. Resp. 33–34. Relying on Petitioner's contentions that "Tela's attempts to apply those patents to Intel's products would render Tela's patents invalid because Intel's technology was developed by Intel first" (Ex. 2002 ¶ 44; Ex. 2003 ¶ 44; Ex. 2007 ¶ 50), and the fact that "[t]he Federal Circuit has repeatedly held that there is no practicing the prior art defense to literal infringement," Patent Owner contends that "Intel's argument cannot be a non-infringement position." Prelim. Resp. 33. Patent Owner further contends that "the Federal Circuit has expressed the view that an assertion by a party accused of infringement that it is practicing the prior art is only appropriate as an invalidity position" on the basis that the court "has held that the 'practicing the prior art'

assertion may be utilized to argue that 'if a claim term [is] broadly interpreted to read on an accused device, then this same broad construction will read on the prior art,' making the claim invalid." *Id.* at 34 (citing *01 Communique Lab., Inc. v. Citrix Sys., Inc.*, 889 F.3d 735, 742 (Fed. Cir. 2018)).

Patent Owner's argument that Intel's pleadings amount to a "practicing the prior art argument" fails to support its position that the § 315(a)(1) bar is triggered. Whatever the merit of such a non-infringement contention based on the proper construction of the claims, Patent Owner does not provide us with a sound basis to consider it a pleading for invalidity. *See generally* Prelim. Resp.; Sur-Reply. The Federal Circuit's decision in *01 Communique* sets forth that "an accused infringer cannot defeat a claim of literal infringement or establish invalidity merely by pointing to similarities between an accused product and the prior art." *01 Communique*, 889 F.3d at 742. And, while *01 Communique* allows that a litigant can argue invalidity on the basis that a broad construction that reads on the accused device would read on the prior art, it does not clearly stand for the proposition Patent Owner sets forth—that an argument contending, in effect, that a broad construction is erroneous because it would read on the prior art is necessarily a pleading of invalidity. *Id.* Moreover, as discussed above, Patent Owner's own counsel appears to have rejected the notion that it does. Ex. 2005, 6:16–19 ("They've—in Your Honor's prior order you had indicated—I think you believed that Intel had alleged invalidity of patents. They've gone out of their way not to allege invalidity of the patents.").

For the foregoing reasons, we conclude that the Petition is not barred under § 315(a)(1).

2. 35 U.S.C. § 314(a)

Patent Owner contends that the Board should deny institution because it would be an inefficient use of the Board's resources when Petitioner is pursuing the same relief in other proceedings. Prelim. Resp. 34–46. Patent Owner argues that Petitioner's strategy involving both the NDCA Action and the ITC Proceeding makes instituting an *inter partes* review contrary to "mak[ing] the patent system more efficient by the use of post-grant review procedures." *Id.* at 38 (citing *General Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16 (PTAB Sept. 6, 2017) (designated precedential as to § II.B.4.i)).

Patent Owner argues that the NDCA Action involves the same invention and the same prior art references. *Id.* at 17 (citing Ex. 2019), 35–36. Patent Owner also argues that the NDCA Action is "significantly advanced." *Id.* at 36 (citing *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018)). Patent Owner also argues that this proceeding would not be an efficient alternative to litigation. *Id.* at 37–42. Patent Owner contends that "[a]ll discovery in the NDCA action (fact and expert) will be completed by May 15, 2020, at least six months before any final decision on this Petition under the normal timing rules." Sur-Reply 6. Patent Owner further contends that "[t]he fact that the Final Written Decision will be issued on this Petition (if instituted) prior to the currently scheduled NDCA Action trial is irrelevant and ignores the true status of the NDCA Action." *Id.* And Patent Owner faults Petitioner for failing to seek a stay in the NDCA Action. *Id.*; Prelim. Resp. 3, 12, 41.

Petitioner responds that Patent Owner fails to identify "any decision in which discretionary denial was predicated on fact patterns similar to the present case." Reply 7. As Petitioner sets forth, "the crucial fact [is] that, as

currently scheduled, the Final Written Decision in this case (assuming institution) would issue ***before*** the currently-scheduled jury trial, which starts in March 2021." *Id.* (citing Ex. 1040, 8). Thus, in addition to other differences Petitioner highlights between this case and those on which Patent Owner relies, an *inter partes* review in this case would result in a final written decision prior to trial in the NDCA Action and would, thereby, "resolve complex issues that otherwise would need to be litigated at trial and addressed by a jury." *Id*.

Moreover, Patent Owner's arguments grounded on the failure of Petitioner to seek a stay in the NDCA Action upon filing the IPR Petitions (Prelim. Resp. 12; Sur-Reply 1, 6) are unpersuasive because they fail to establish that parties are not free to seek a stay after institution of an *inter partes* proceeding. The further conclusory argument that "this Petition will not provide an efficient alternative to the district court litigation" because "the NDCA Action will deal with all [six Patent Owner] patents in a single proceeding, so the issues common to those patents will be resolved simultaneously" (Sur-Reply 6) is unpersuasive, because it is unsupported by any reasoning or evidence suggesting that the district court's single proceeding addressing these six patents is more efficient than the *inter partes* review proceedings that would address the same six patents (*see generally* Prelim. Resp.; Sur-Reply).

Patent Owner also points to the ITC Proceeding, noting that Petitioner asserted invalidity of the '966 patent there, relying on the same prior art and contentions that are set forth in the Petition. Prelim. Resp. 13–15, 36. Although acknowledging that the '966 patent was terminated from the ITC Proceeding, and that Petitioner's invalidity arguments in that proceeding will not go to hearing, Patent Owner relies on "Intel's simultaneous pursuit of

duplicative invalidity theories in the ITC as part of detailing Intel's overall pattern of wasteful and inefficient pursuit of the same invalidity theories in multiple forums." *Id*. at 15. Patent Owner also argues that "invalidity determinations in the ITC have weight and will help resolve the invalidity grounds raised by Intel." *Id.* at 40.

In response, Petitioner rightfully highlights that the '966 patent has been terminated from the ITC Proceeding, and was, accordingly, irrelevant to addressing the issue of validity when Patent Owner filed its Preliminary Response. Reply 10. Patent Owner also relies on the ITC Proceeding as evidencing "Intel's overall pattern of wasteful and inefficient pursuit of the same invalidity theories in multiple forums" (Prelim. Resp. 15), but Patent Owner offers no cogent argument with that assertion, or elsewhere, for denying institution where the '966 patent has been terminated from the ITC Proceeding (*see generally* Prelim. Resp.; Sur-Reply).

Patent Owner also points to Petitioner's filing of a number of petitions seeking an *inter partes* review of the '966 patent, and other patents. Prelim. Resp. 15, 42–46. Patent Owner argues that "Intel's strategy of filing multiple overlapping petitions conflicts with and is harmful to efficient administration by the Board." *Id.* at 42. Patent Owner further argues that the Board should deny at least one of the two remaining petitions challenging the '966 patent. Paper 17, 2–5.

Patent Owner, however, fails to explain how filing a large number of petitions challenging a number of different patents supports denying institution of every petition, including this one. *See generally* Prelim. Resp.; Sur-Reply; Paper 17. The total number of Patent Owner's patents Petitioner is challenging is not a sufficient reason to deny institution in this particular proceeding. "[R]ecogniz[ing] the potential for abuse of the review process

by repeated attacks on patents," the Board has enumerated factors that guide its discretion as to whether to deny institution under § 314(a), "especially as to 'follow-on' petitions challenging the same patent as challenged previously in an IPR . . . proceeding." Patent Trial and Appeal Board Consolidated Trial Practice Guide 56 (Nov. 2019), *available at* https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf (quoting *General Plastic*, IPR2016-01357, Paper 19 at 16–17). Perhaps sixteen petitions were filed in total (Prelim. Resp. 45), but only the 1220 IPR petition, the 1221 IPR petition, and this Petition challenge the '966 patent. The 1221 IPR petition has been withdrawn. Patent Owner's concerns regarding abuse of the review process grounded on multiple petitions directed to the same patent are moot, in any event, because we have exercised our statutory discretion (delegated from the Director) to deny institution of an *inter partes* review in the 1220 IPR. *See Intel Corp. v. Tela Innovations, Inc.*, IPR2019-01220, Paper 19 (PTAB Jan. 30, 2020).

For the foregoing reasons, we decline Patent Owner's request to exercise our discretion under 35 U.S.C. § 314(a) to deny review.

E. Asserted Obviousness of Claims 2, 31–33, and 35

Petitioner argues that claims 2, 31–33, and 35 are obvious over Ichiryu. Pet. 29–62.

1. Ichiryu

Ichiryu is a patent titled "Cell, Standard Cell, Standard Cell Library, a Placement Method Using Standard Cell, and a Semiconductor Integrated Circuit." Ex. 1013, code (54). Ichiryu relates to "a standard cell, a standard cell library and a placement method of standard cells for higher integration and area reduction." *Id.* at 1:9–11. Ichiryu describes challenges associated with the placement of standard cells within a grid layout. *Id.* at 1:66–2:22.

One such challenge is, as the miniaturization of the grid layout increases, a precision in a finished dimension of a gate electrode is deteriorated due to an optical proximity effect that occurs when intervals between gate electrodes and gate lengths of gate electrode are irregular in their patterns. *Id.* at 2:23–27. Such a deterioration causes a decrease in a yield ratio (*i.e.*, an increase in inconstant performance of transistors of the semiconductor integrated circuit). *Id.* at 2:27–32. In order to address this problem, Ichiryu describes a layout of a standard cell that includes dummy gate electrodes, resulting in a regular gate length and gate interval. *Id.* at 2:32–64. Figure 11 of Ichiryu, shown below, illustrates an example standard cell layout.

F I G. 11

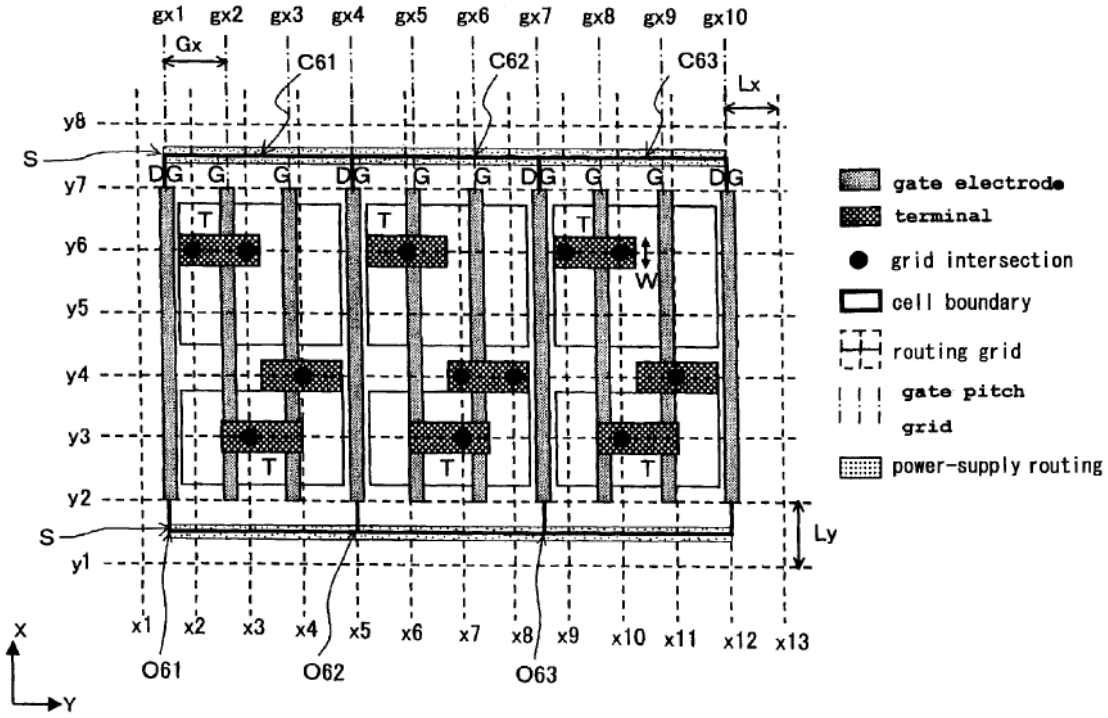

Figure 11 illustrates a layout of standard cells. *Id.* at 8:64–65. In reference to Figure 11, Ichiryu describes that: x1–x13 denote routing grids for the automatic placement and routing disposed in parallel with the Y direction and adjacent to one another in the X direction; y1–y8 denote routing grids

disposed in parallel with the X direction and adjacent to one another in the Y direction; gx1–gx10 denote grids of gate pitches for the automatic placement and routing disposed in parallel with the Y direction and adjacent to one another in the X direction; C61, C62, and C63 are standard cells; O61, O62, and O63 are respective origins of the standard cells C61, C62, and C63; T denotes a terminal capable of transmitting an input signal or an output signal of the standard cell; G denotes a gate electrode; and DG denotes a dummy gate electrode. *Id.* at 14:32–44. As described in Ichiryu, in standard cells C61, C62, and C63, "gate lengths and gate intervals of the gate electrode G and dummy gate electrode DG are constant." *Id.* at 14:45–51.

2. Analysis

Petitioner, relying heavily on various annotated versions of Ichiryu's Figure 11, contends that Ichiryu discloses the limitations of challenged independent claim 2. Pet. 29–48. Petitioner further argues that, to the extent Ichiryu does not explicitly disclose the limitations of claim 2, one of ordinary skill in the art would have understood various aspects of Ichiryu are formed in a particular manner or exist in a particular configuration. *Id.; see, e.g., id.* at 31–32, 33–34.

More particularly, with respect to claim 2, Petitioner argues that Ichiryu discloses:

Preamble: "An integrated circuit device, comprising:" (Pet. 29–30 (relying on Ex. 1013; Ex. 1002 ¶ 310));

Element 2.1: "a substrate region that forms part of an overall substrate of the integrated circuit device," (Pet. 30–32 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 311–314));

Element 2.2a: "a gate electrode level region that forms part of an overall gate electrode level of the integrated circuit device, the gate electrode

level region formed above and over the substrate region, wherein the gate electrode level region includes a plurality of linear conductive segments" (Pet. 32–37 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 315–324)); Petitioner further argues that, under both Petitioner's and Patent Owner's proposed constructions of "linear conductive segments," the gate structures in Ichiryu's Figure 11 meet this limitation (*id.* at 35 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶ 322));

Element 2.2b: "each formed to have a respective length and a respective width as measured parallel to the substrate region, wherein a size of the length of a given linear conductive segment is greater than or equal to a size of the width of the given linear conductive segment," (Pet. 37–39 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 325–329));

Element 2.2c: "wherein the plurality of linear conductive segments are formed to have their lengths extend in a first direction in a parallel manner, and" (Pet. 39–40 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 330–331)):

Element 2.3: "wherein the plurality of linear conductive segments are positioned in a side-by-side manner according to a substantially equal centerline-to-centerline spacing as measured in a second direction perpendicular to the first direction, and" (Pet. 40–42 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 332–334));

Element 2.4: "wherein the plurality of linear conductive segments include a first linear conductive segment defined to form both a gate electrode of a first transistor of a first transistor type and a gate electrode of a first transistor of a second transistor type, and" (Pet. 42–44 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 335–339));

Element 2.5: "wherein the plurality of linear conductive segments include a second linear conductive segment that does not form a gate electrode of a transistor device, and" (Pet. 44–46 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 340–341)); and

Element 2.6: "wherein the plurality of linear conductive segments include a third linear conductive segment defined to form both a gate electrode of a second transistor of the first transistor type and a gate electrode of a second transistor of the second transistor type." (Pet. 46–48 (relying on Ex. 1013, Fig. 11; Ex. 1002 ¶¶ 342–343)).

Patent Owner does not present arguments addressing the specific merits of Petitioner's ground in the Preliminary Response. Thus, having reviewed Petitioner's assertions regarding independent claim 2, as well as the cited portions of Ichiryu, we determine that Petitioner has demonstrated a reasonable likelihood of establishing that independent claim 2 would have been obvious over Ichiryu.

We have reviewed Petitioner's argument and evidence that Ichiryu discloses the limitations of dependent claims 31–33 and 35. Pet. 48–62. Patent Owner does not address Petitioner's challenges to the dependent claims. Based on the preliminary record before us, we also find that Petitioner's argument and evidence is sufficient to show a reasonable likelihood Petitioner would prevail in proving unpatentability of dependent claims 31–33 and 35.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the '966 patent. Thus, we institute an *inter partes* review on all challenged claims and on the ground presented.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review is instituted with respect to the ground asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this decision.

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